Incializácia, konfigurácia, čiastočná rekonfigurácia FPGA obvodov

Obsah

- spôsoby inicializácie (aktívna, pasívna, sériová paralelná),
- typické formáty inicializačných súborov,
- technológia hraničných testov (Boundary Scan Technology), norma IEEE JTAG 1149.1,
- perspektívy rozvoja testovacích techník (signal tap)

Preberaná problematika bude demonštrovaná na vybraných produktoch firmy Altera. Analyzované princípy sú však používané aj inými výrobcami obvodov FPGA.

Konfigurácia FPGA

Čítanie konfiguračných dát z FLASH pamäte
Dekompresia údajov (ak bola použitá)
Vyslanie konfiguračných údajov na príslušný pin(y)
Detekcia chýb

Spôsoby konfiguácie obvodov Altera

Passive Serial – konfiguračné dáta sú prenášané 1bit/hodinový cyklus
Active Serial – konfiguračné dáta sú prenášané 1bit/hodinový cyklus
Passive Parallel Synchronous – 8 datových + 8 hodinových na serializáciu dát
Fast Passive Parallel – konfiguračné dáta sú prenášané 1bajt/hodinový cyklus
Passive Parallel Asynchronous – prenos 8 datových riadia asynchrónne riadiace signály
Passive Serial Asynchronous – prenos 1 bit riadia asynchrónne riadiace signály
JTAG – konfiguračné dáta sú prenášané sériovým JTAG rozhraním

Table 1–2. Configuration Schemes

Configuration Scheme	Typical Use
Passive Serial (PS)	Configuration with the enhanced configuration devices (EPC16, EPC8, and EPC4), EPC2, EPC1, EPC1441 configuration devices, serial synchronous microprocessor interface, the USB Blaster USB Port Download Cable, MasterBlaste™r communications cable, ByteBlaster™ II parallel download cable or ByteBlasterMV™ parallel port download cable.
Active Serial (AS)	Configuration with the serial configuration devices (EPCS1 and EPCS4).
Passive Parallel Synchronous (PPS)	Configuration with a parallel synchronous microprocessor interface.
Fast Passive Parallel (FPP)	Configuration with an enhanced configuration device or parallel synchronous microprocessor interface where 8 bits of configuration data are loaded on every clock cycle. Eight times faster than PPS.
Passive Parallel Asynchronous (PPA)	Configuration with a parallel asynchronous microprocessor interface. In this scheme, the microprocessor treats the target device as memory.
Passive Serial Asynchronous (PSA)	Configuration with a serial asynchronous microprocessor interface.
Joint Test Action Group (JTAG)	Configuration through the IEEE Std. 1149.1 (JTAG) pins. (1)

Špeciálne konfiguračné pamäte

Enhanced configuration devices (široko rekonfigurovateľné, vysoká cena, veľké puzdro)

- 1-bit passive serial (PS)
- 2-bit passive serial
- 4-bit passive serial
- 8-bit passive serial
- Fast passive parallel (FPP)

Serial configuration devices (nízka cena, len pre vybrané FPGA - Cyclone, Stratix II)

- Active serial

Table 1–1. Altera Configuration Devices

Device	Memory Size (bits)	On-Chip Decompression Support	ISP Support	Daisy Chain Support	Reprogrammable	Operating Voltage (V)
EPC16	16,777,216	Yes	Yes	No	Yes	3.3
EPC8	8,388,608	Yes	Yes	No	Yes	3.3
EPC4	4,194,304	Yes	Yes	No	Yes	3.3
EPCS64	67,108,864 *(1)*	No	No *(2)*	No	Yes	3.3
EPCS16	16,777,216 *(1)*	No	No *(2)*	No	Yes	3.3
EPCS4	4,194,304	No	No *(2)*	No	Yes	3.3
EPCS1	1,048,576	No	No *(2)*	No	Yes	3.3
EPC2	1,695,680	No	Yes	Yes	Yes	5.0 or 3.3
EPC1	1,046,496	No	No	Yes	No	5.0 or 3.3
EPC1441	440,800	No	No	No	No	5.0 or 3.3

Notes to Table 1–1:

(1) This information is preliminary.

(2) The EPCS device can be re-programmed in system by an external microprocessor using SRunner. For more information about SRunner see the *SRunner: in Embedded Solution for EPCS Programming White Paper* on the Altera web site at **www.altera.com**.

Prehľad konfiguračných metód a ich podpora v rôznych rodinách obvodov Altera

- Aktívna (FPGA generuje riadiace a synchronizačné signály)
- Pasívna (konfiguračné zariadenie (uP, konf. pamäť) generuje riadiace signály)
- JTAG

Table 1–1. Configuration Scheme Device Family Support

Configuration Scheme	Device Family									
	Stratix II	Stratix, Stratix GX	Cyclone II	Cyclone	APEX II	APEX 20K, APEX 20KE, APEX 20KC	Mercury	ACEX 1K	FLEX 10K, FLEX 10KE, FLEX 10KA	FLEX 6000
Passive Serial (PS)	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
Active Serial (AS)	✓		✓	✓						
Fast Passive Parallel (FPP)	✓	✓			✓					
Passive Parallel Synchronous (PPS)						✓	✓	✓	✓	
Passive Parallel Asynchronous (PPA)	✓	✓			✓	✓	✓	✓	✓	
Passive Serial Asynchronous (PSA)										✓
Joint Test Action Group (JTAG)	✓	✓	✓	✓	✓	✓	✓	✓	✓	*(1)*

Enhanced Configuration Devices (EPC4, EPC8, EPC16)

- Single-chip configuration solution for Stratix® series, Cyclone™ series, APEX™ II, APEX 20K (including APEX 20K, APEX 20KC, and APEX 20KE), Mercury™, ACEX® 1K, and FLEX® 10K (FLEX 10KE and FLEX 10KA) devices
- Contains 4-, 8-, and 16-Mbit flash memories for configuration data storage
- On-chip decompression feature almost doubles the effective configuration density
- Standard flash die and a controller die combined into single stacked chip package
- External flash interface supports parallel programming of flash and external processor access to unused portions of memory
- Flash memory block/sector protection capability via external flash interface
- Supported in EPC16 and EPC4 devices
- Page mode support for remote and local reconfiguration with up to eight configurations for the entire system
- Compatible with Stratix series Remote System Configuration feature
- Supports byte-wide configuration mode fast passive parallel (FPP);8-bit data output per `DCLK` cycle
- Supports true n-bit concurrent configuration (n = 1, 2, 4, and 8) of Altera FPGAs
- Pin-selectable 2-ms or 100-ms power-on reset (POR) time
- Configuration clock supports programmable input source and frequency synthesis
    - Multiple configuration clock sources supported (internal oscillator and external clock input pin)
    - External clock source with frequencies up to 133 MHz
    - Internal oscillator defaults to 10 MHz; Programmable for higher frequencies of 33, 50, and 66 MHz
    - Clock synthesis supported via user programmable dividecounter
- Available in the 100-pin plastic quad flat pack (PQFP) and the 88-pin Ultra FineLine BGA® packages
- Vertical migration between all devices supported in the 100-pin PQFP package
- Supply voltage of 3.3 V (core and I/O)
- Hardware compliant with IEEE Std. 1532 in-system programmability (ISP) specification
- Supports ISP via Jam Standard Test and Programming Language (STAPL)
- Supports Joint Test Action Group (JTAG) boundary scan
- `nINIT_CONF` pin allows private JTAG instruction to initiate FPGA configuration
- Internal pull-up resistor on `nINIT_CONF` always enabled
- User programmable weak internal pull-up resistors on `nCS` and `OE` pins
- Internal weak pull-up resistors on external flash interface address and control lines, bus hold on data lines
- Standby mode with reduced power consumption

Figure 2–1. Enhanced Configuration Device Block Diagram

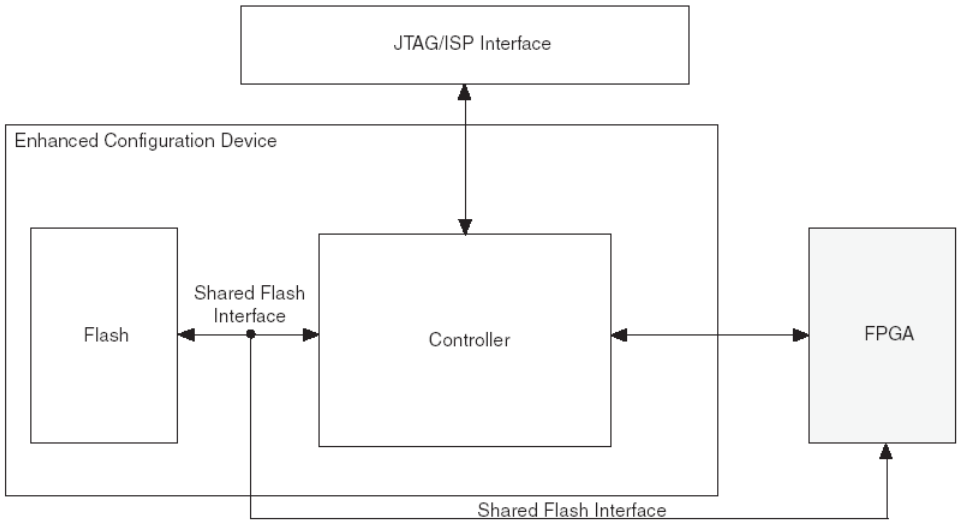


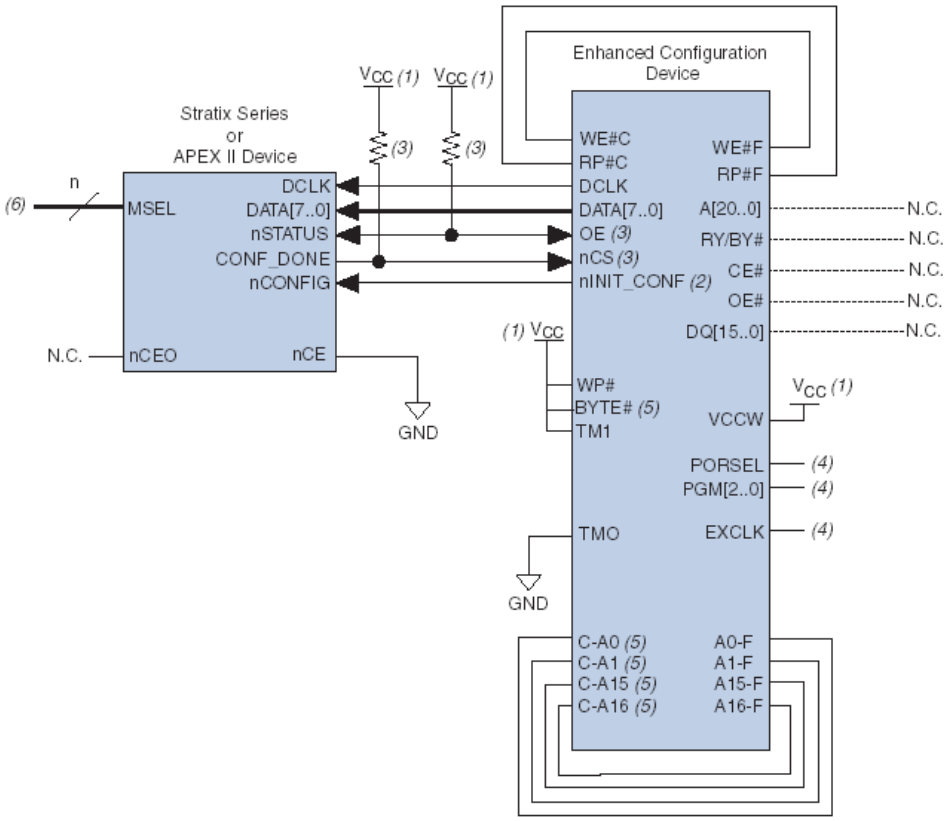
Table 2–3. Configuration Signals

Enhanced Configuration Device Pin	Altera FPGA Pin	Description
DATA[]	DATA[]	Configuration data transmitted from the configuration device to the FPGA, which is latched on the rising edge of DCLK.
DCLK	DCLK	Configuration device generated clock used by the FPGA to latch configuration data provided on the DATA[] pins.
nINIT_CONF	nCONFIG	Open-drain output from the configuration device that is used to initiate FPGA reconfiguration using the initiate configuration (INIT_CONF) JTAG instruction. This connection is not needed if the INIT_CONF JTAG instruction is not needed. If nINIT_CONF is not connected to nCONFIG, nCONFIG must be tied to V_{CC} either directly or through a pull-up resistor.
OE	nSTATUS	Open-drain bidirectional configuration status signal, which is driven low by either device during POR and to signal an error during configuration. Low pulse on OE resets the enhanced configuration device controller.
nCS	CONF_DONE	Configuration done output signal driven by the FPGA.

Spôsoby konfigurácie

Fast Passive Parallel (FPP) Configuration (napr. Stratix a APEX II)

Figure 2–2. FPP Configuration



Notes to Figure 2–2:

(1) The V_{CC} should be connected to the same supply voltage as the configuration device.

(2) The `nINIT_CONF` pin is available on enhanced configuration devices and has an internal pull-up resistor that is always active. This means an external pull-up resistor is not required on the `nINIT_CONF`/`nCONFIG` line. The `nINIT_CONF` pin does not need to be connected if its functionality is not used. If `nINIT_CONF` is not used, `nCONFIG` must be pulled to V_{CC} either directly or through a resistor.

(3) The enhanced configuration devices' `OE` and `nCS` pins have internal programmable pull-up resistors. If internal pull-up resistors are used, external pull-up resistors should not be used on these pins. The internal pull-up resistors are used by default in the Quartus® II software. To turn off the internal pull-up resistors, check the **Disable nCS and OE pull-ups on configuration device** option when generating programming files.

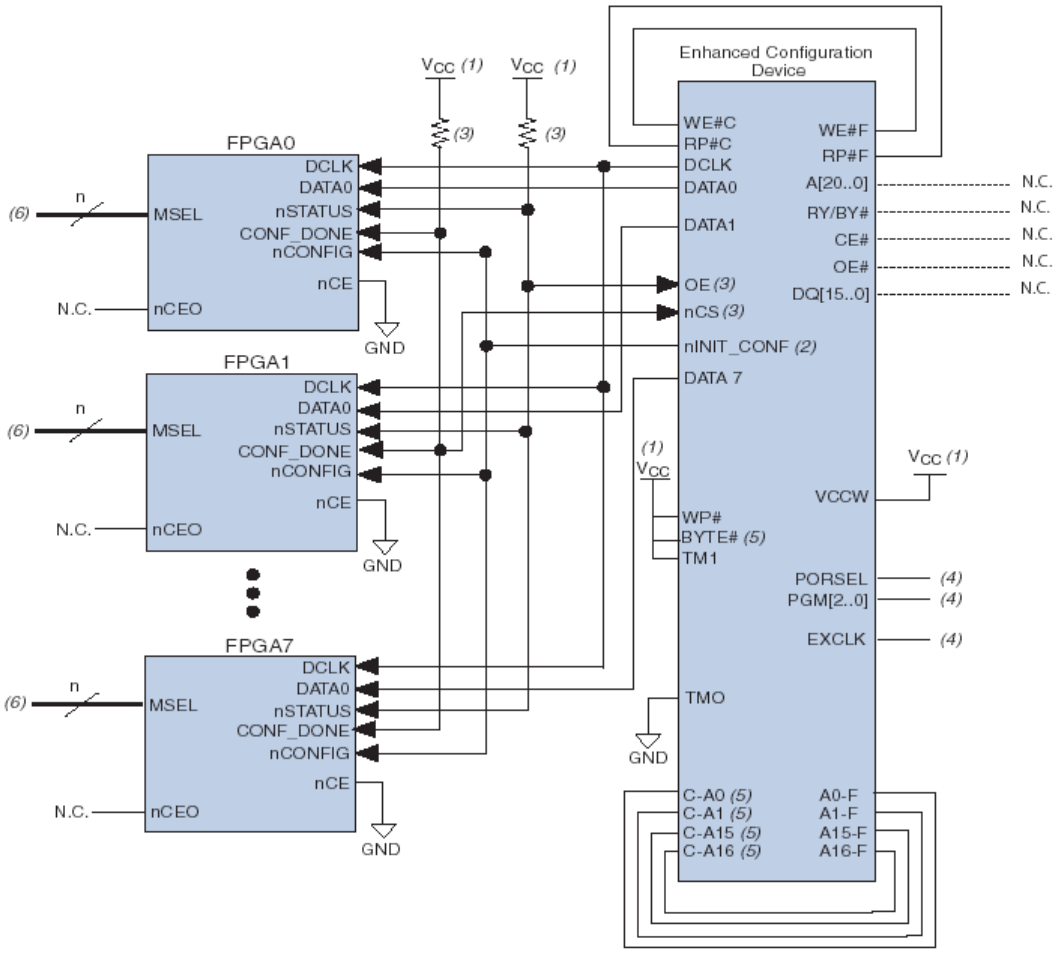
(4) For `PORSEL`, `PGM[]`, and `EXCLK` pin connections, refer to Table 2–9.

(5) In the 100-pin PQFP package, you must externally connect the following pins: `C-A0` to `F-A0`, `C-A1` to `F-A1`, `C-A15` to `F-A15`, `C-A16` to `F-A16`, and `BYTE#` to V_{CC}. Additionally, you must make the following pin connections in both 100-pin PQFP and 88-pin Ultra FineLine BGA packages: `C-RP#` to `F-RP#`, `C-WE#` to `F-WE#`, `TM1` to V_{CC}, `TM0` to GND, and `WP#` to V_{CC}.

(6) Connect the FPGA `MSEL[]` input pins to select the FPP configuration mode. For details, refer to the appropriate FPGA family chapter in the Configuration Handbook.

Passive Serial (PS) Configuration
- podobná ako PS, použité iba DATA[0]
Concurrent Configuration viacerých FPGA (FPGA chain) v PS mode

Figure 2–3. Concurrent Configuration of Multiple FPGAs in PS Mode (n = 8)



Notes to Figure 2–3:

(1) Connect V_{CC} to the same supply voltage as the configuration device.

(2) The `nINIT_CONF` pin is available on enhanced configuration devices and has an internal pull-up resistor that is always active. This means an external pull-up resistor is not required on the `nINIT_CONF`/`nCONFIG` line. The `nINIT_CONF` pin does not need to be connected if its functionality is not used. If `nINIT_CONF` is not used, `nCONFIG` must be pulled to V_{CC} either directly or through a resistor.

(3) The enhanced configuration devices' `OE` and `nCS` pins have internal programmable pull-up resistors. If internal pull-up resistors are used, external pull-up resistors should not be used on these pins. The internal pull-up resistors are used by default in the Quartus II software. To turn off the internal pull-up resistors, check the **Disable nCS and OE pull-ups on configuration device** option when generating programming files.

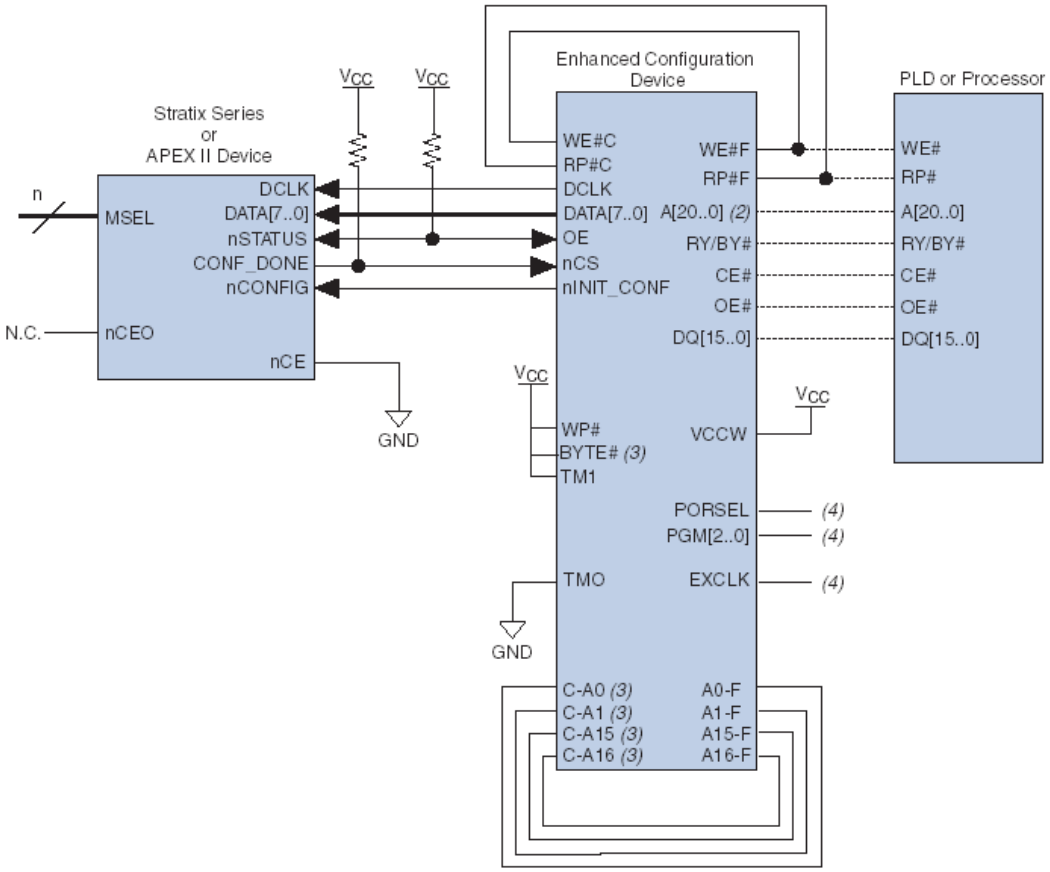
(4) For `PORSEL`, `PGM[]`, and `EXCLK` pin connections, refer to Table 2–9.

(5) In the 100-pin PQFP package, you must externally connect the following pins: `C-A0` to `F-A0`, `C-A1` to `F-A1`, `C-A15` to `F-A15`, `C-A16` to `F-A16`, and `BYTE#` to V_{CC}. Additionally, you must make the following pin connections in both 100-pin PQFP and 88-pin Ultra FineLine BGA packages: `C-RP#` to `F-RP#`, `C-WE#` to `F-WE#`, `TM1` to V_{CC}, `TM0` to GND, and `WP#` to V_{CC}.

(6) Connect the FPGA `MSEL[]` input pins to select the PS configuration mode. For details, refer to the appropriate FPGA family chapter in the Configuration Handbook.

External FLASH interface

Figure 2–4. FPP Configuration with External Flash Interface *Note (1)*



Notes to Figure 2–4:

(1) For external flash interface support in EPC8 enhanced configuration device, contact Altera Applications.

(2) Pin `A20` in EPC16 devices, pins `A20` and `A19` in EPC8 devices, and pins `A20`, `A19`, and `A18` in EPC4 devices should be left floating. These pins should not be connected to any signal, i.e., they are no-connect pins.

(3) In the 100-pin PQFP package, you must externally connect the following pins: `C-A0` to `F-A0`, `C-A1` to `F-A1`, `C-A15` to `F-A15`, `C-A16` to `F-A16`, and `BYTE #` to V_{CC}. Additionally, you must make the following pin connections in both 100-pin PQFP and 88-pin Ultra FineLine BGA packages: `C-RP#` to `F-RP#`, `C-WE#` to `F-WE#`, `TM1` to V_{CC}, `TM0` to GND, and `WP#` to V_{CC}.

(4) For `PORSEL`, `PGM[]`, and `EXCLK` pin connections, refer to Table 2–9.

Real-time decompression

The decompression feature supported in the enhanced configuration devices is different from the decompression feature supported by the Stratix II FPGAs and the Cyclone series. When configuring Stratix II FPGAs or the Cyclone series using enhanced configuration devices, Altera recommends enabling decompression in Stratix II FPGAS or the Cyclone series only for faster configuration.

Table 2–5. Stratix Compression Ratios *Note (1)*

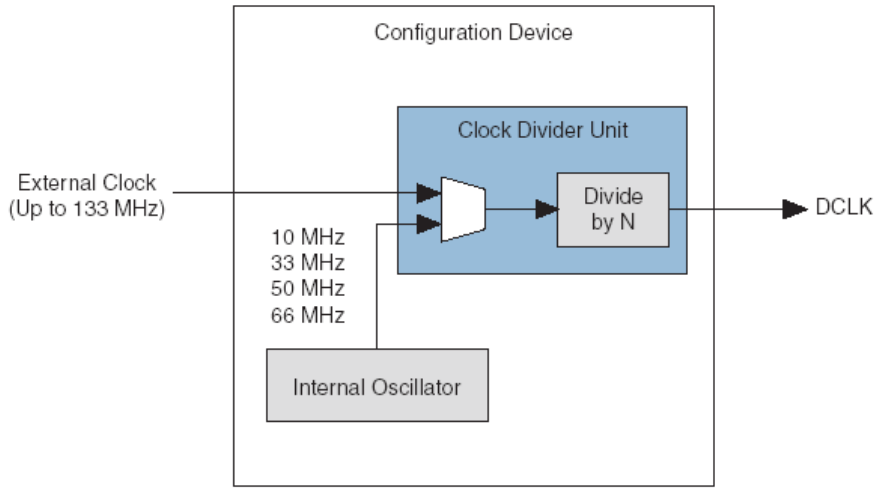
	Minimum	Average
Logic Utilization	98%	64%
Compression Ratio	1.9	2.3
% Size Reduction	47%	57%

Note to Table 2–5:

(1) These numbers are preliminary. They are intended to serve as a guideline, not a specification.

Programmable Configuration Clock (DCLK)

Figure 2–5. Clock Divider Unit



Flash In-System Programming (ISP)

- pomocou JTAG rozhrania
- pomocou externého flash rozhrania (16 bitová datová zbernica

100000 programovacích cyklov

Serial Configuration Devices (EPCS1, EPCS4, EPCS16, EPCS64)

- 1-, 4-, 16-, and 64-Mbit flash memory devices that serially configure Stratix® II FPGAs and the Cyclone™ series FPGAs using the active serial (AS) configuration scheme
- Easy-to-use four-pin interface
- Low cost, low pin count and non-volatile memory
- Low current during configuration and near-zero standby mode current
- 3.3-V operation
- Available in 8-pin and 16-pin small outline integrated circuit (SOIC) package
- Enables the Nios® processor to access unused flash memory through AS memory interface
- Re-programmable memory with more than 100,000 erase/program cycles
- Write protection support for memory sectors using status register bits
- In-system programming support with SRunner software driver
- In-system programming support with USB Blaster™ or ByteBlaster™ II download cables
- Additional programming support with the Altera® Programming Unit (APU) and programming hardware from BP Microsystems, System General, and other vendors
- Software design support with the Altera Quartus® II development system for Windows-based PCs as well as Sun SPARC station and HP 9000 Series 700/800
- Delivered with the memory array erased (all the bits set to `1`)

Príklad veľkostí konfiguračných súborov v najnovších obvodoch Stratiix II a Cyclone II

Table 4–2. Serial Configuration Device Support for Stratix II Devices

Stratix II Device	Raw Binary File Size (Bits) *(1)*	Serial Configuration Device	
		EPCS16	EPCS64
EP2S15	5,000,000	✓	✓
EP2S30	10,100,000	✓	✓
EP2S60	17,100,000	✓ *(2)*	✓
EP2S90	27,500,000		✓
EP2S130	39,600,000		✓
EP2S180	52,400,000		✓

Notes to Table 4–2:

(1) These are preliminary, uncompressed file sizes.

(2) This is with the Stratix II compression feature enabled.

Table 4–2. Serial Configuration Device Support for Stratix II Devices

Stratix II Device	Raw Binary File Size (Bits) *(1)*	Serial Configuration Device	
		EPCS16	EPCS64
EP2S15	5,000,000	✓	✓
EP2S30	10,100,000	✓	✓
EP2S60	17,100,000	✓ *(2)*	✓
EP2S90	27,500,000		✓
EP2S130	39,600,000		✓
EP2S180	52,400,000		✓

Notes to Table 4–2:

(1) These are preliminary, uncompressed file sizes.

(2) This is with the Stratix II compression feature enabled.

Figure 4–1. Serial Configuration Device Block Diagram

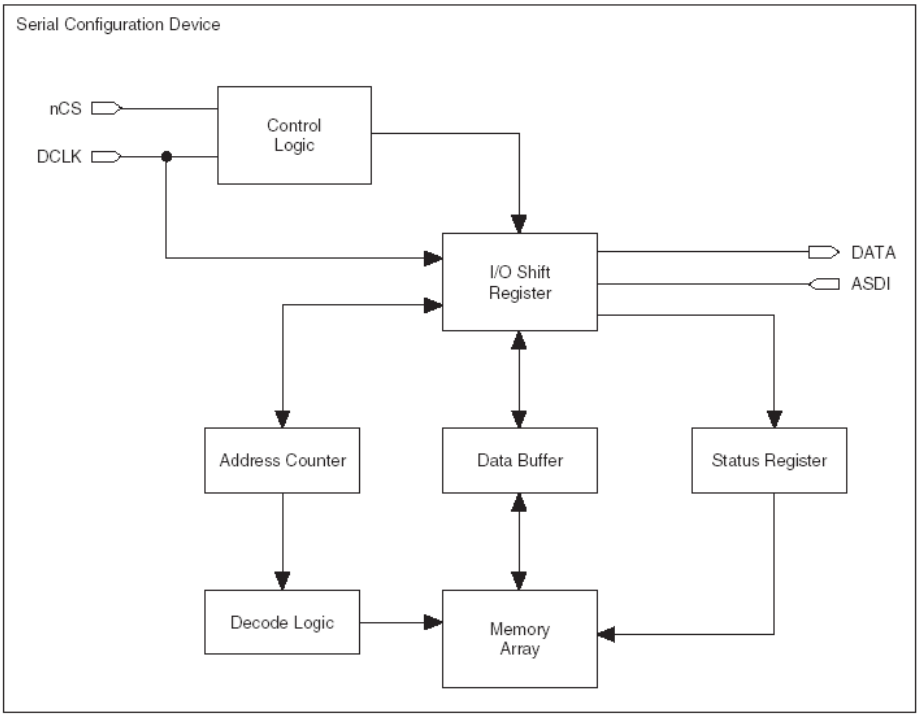


Table 4–22. Serial Configuration Device Pin Description

Pin Name	Pin Number	Pin Type	Description
DATA	2	Output	The DATA output signal transfers data serially out of the serial configuration device to the FPGA during read/configuration operation. During a read/configuration operations, the serial configuration device is enabled by pulling nCS low. The DATA signal transitions on the falling edge of DCLK.
ASDI	5	Input	The AS data input signal is used to transfer data serially into the serial configuration device. It receives the data that should be programmed into the serial configuration device. Data is latched in the rising edge of DCLK.
nCS	1	Input	The active low chip select input signal toggles at the beginning and end of a valid instruction. When this signal is high, the device is deselected and the DATA pin is tri-stated. When this signal is low, it enables the device and puts the device in an active mode. After power up, the serial configuration device requires a falling edge on the nCS signal before beginning any operation.
DCLK	6	Input	DCLK is provided by the FPGA. This signal provides the timing of the serial interface. The data presented on ASDI is latched to the serial configuration device, at the rising edge of DCLK. Data on the DATA pin changes after the falling edge of DCLK and is latched into the FPGA on the rising edge.
V_{CC}	3, 7, 8	Power	Power pins connect to 3.3 V.
GND	4	Ground	Ground pin.

Úsporné púzdra

Figure 4–19. Altera Serial Configuration Device 8-Pin SOIC Package Pin-Out Diagram

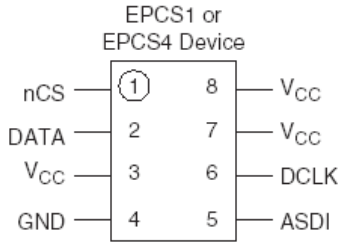
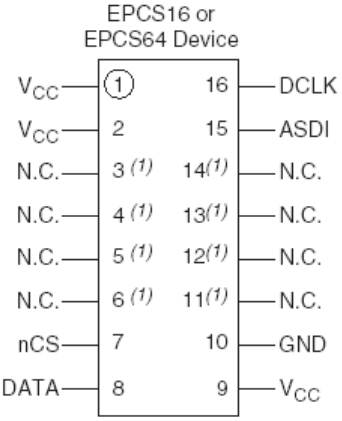


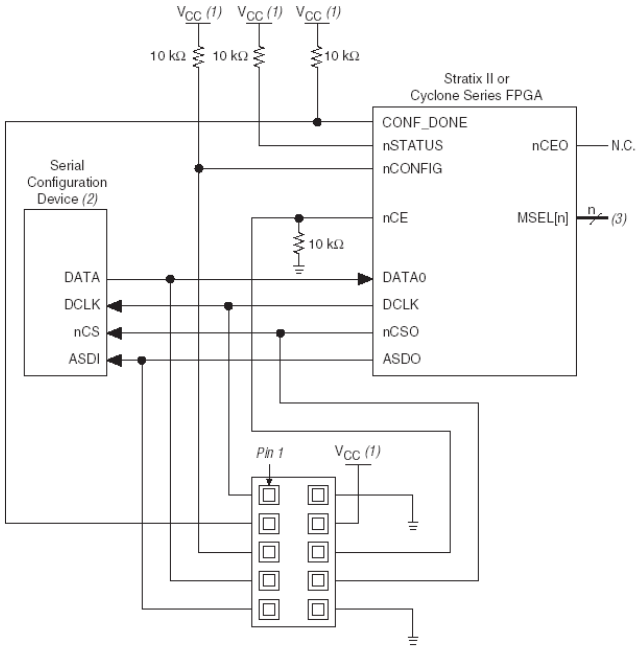
Figure 4–20. Altera Serial Configuration Device 16-Pin SOIC Package Pin-Out Diagram



Note to Figure 4–20:

(1) These pins can be left floating or connected to V_{CC} or GND, whichever is more convenient on the board.

Figure 4–2. FPGA Configuration in AS Mode (Serial Configuration Device Programmed Using Download Cable)



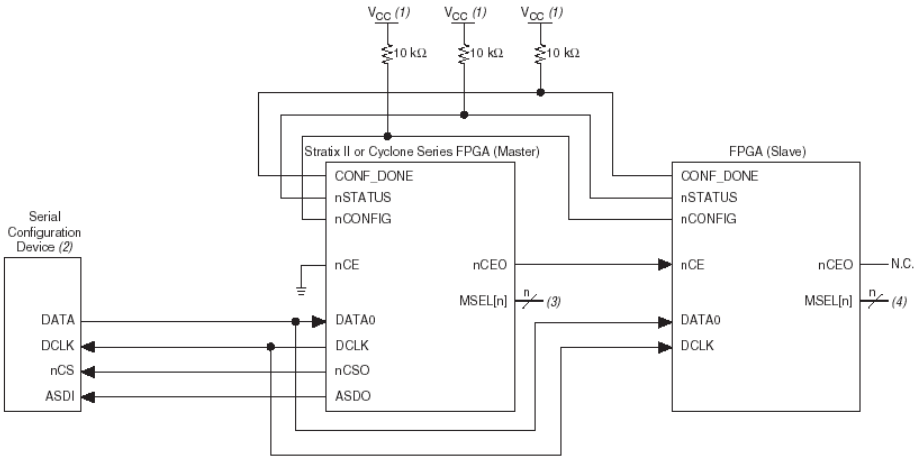
Notes to Figure 4–2:

(1) V_{CC} = 3.3 V.

(2) Serial configuration devices cannot be cascaded.

(3) Connect the FPGA `MSEL[]` input pins to select the AS configuration mode. For details, refer to the appropriate FPGA family chapter in the *Configuration Handbook*.

Figure 4–4. Multiple Devices in AS Mode



Notes to Figure 4–4:

(1) V_{CC} = 3.3 V.

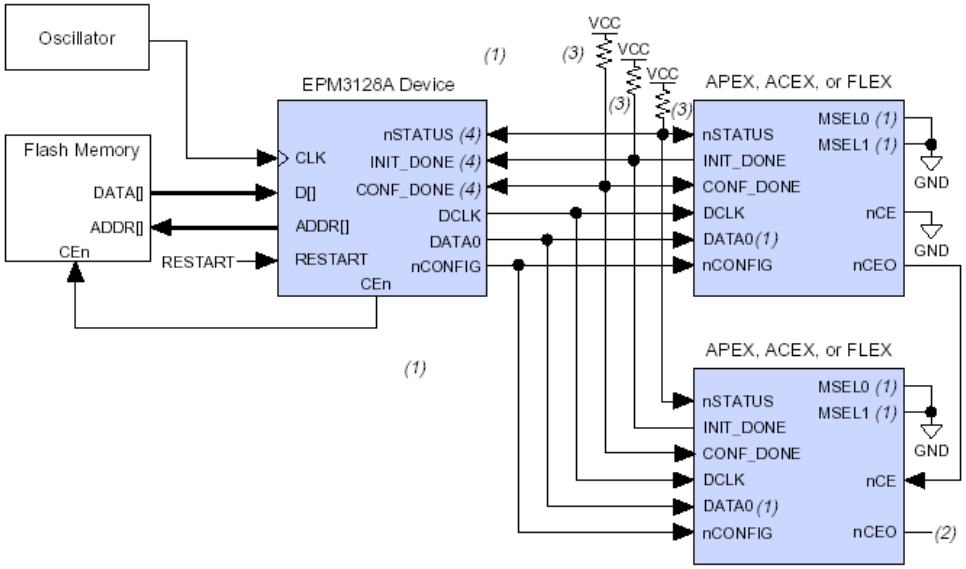
(2) Serial configuration devices cannot be cascaded.

(3) Connect the FPGA `MSEL[]` input pins to select the AS configuration mode. For details, refer to the appropriate FPGA family chapter in the *Configuration Handbook*.

(4) Connect the FPGA `MSEL[]` input pins to select the PS configuration mode. For details, refer to the appropriate FPGA family chapter in the *Configuration Handbook*

Príklad konfigurácie z externej FLASH pamäte (EPM3128 nahradzuje napr. uP)

Figure 1. Device Configuration Using Flash Memory & EPM3128A Device



Notes:

(1) FLEX 6000 devices have a single MSEL pin, which is tied to ground. Additionally, its DATA0 pin is renamed DATA.

(2) The nCEO pin is left unconnected for the last device in the chain.

(3) Pull-up resistors are 1 kΩ except for APEX 20KE devices. For APEX 20KE devices, pull up resistors are 10 kΩ.

(4) The nSTATUS, CONF_DONE, and INIT_DONE pins are open-drain on the APEX, ACEX, and FLEX devices. The corresponding pins on the EPM3128A should also be open_drain.

Konfiguračné formáty (pre obvody Altera)

SRAM Object File (.sof)
Používaný pre PS konfiguráciu pomocou softvéru Quartus II +
- USB Blaster,
- Master Blaster,
- ByteBlaster II,
- EthernetBlaster,
- ByteBlaster MV

Quartus generuje SOF súbor automaticky, všetky ostatné konfiguračné súbory sú vytvárané zo SOF súboru.

Programmer Object File (.pof)
Používaný na programovanie konfiguračných súčiastok pomocou programovacieho hardvéru Altera. Automaticky generovaný Quartusom.

Raw Binary File (.rbf)
Binárny súbor obsahujúci konfiguračné dáta. Dáta môžu byť priamo čítané napr. konfiguračným mikroprocesorom.

Raw Programming Data File (.rpd)
Binárny súbor obsahujúci konfiguračné dáta pre Cyclone FPGA, uložené v konfigurčnej pamäti a používane v AS mode.

Hexadecimal (Intel-Format) file (.hex)
ASCII súbor v Intel-HEX formáte. Používaný napr. externými programátormi, uP, ...

Tabular Text File (.ttf)
ASCII súbor obsahujúci jednotlivé položky oddelené čiarkami. Môže byť priamo začlenený do takmer ľubovoľných zdrojových kódov (napr. ASM, C, ...).

Jam File (.jam)
ASCII súbor v špecializovanom JAM programovacom jazyku, ktorý umožňuje zapísať programovacie informácie, verifikovať a kontrolovať vymazanie súčiastky.

Jam Byte-Code File (.jbc)
Binárna verzia Jam File umožňujúca zapísať programovacie informácie, verifikovať a kontrolovať vymazanie súčiastky.

Príklad využitia Jam Byte-Code player a jednočípového uP na báze Intel 8051

Figure 2. 8051 Architecture

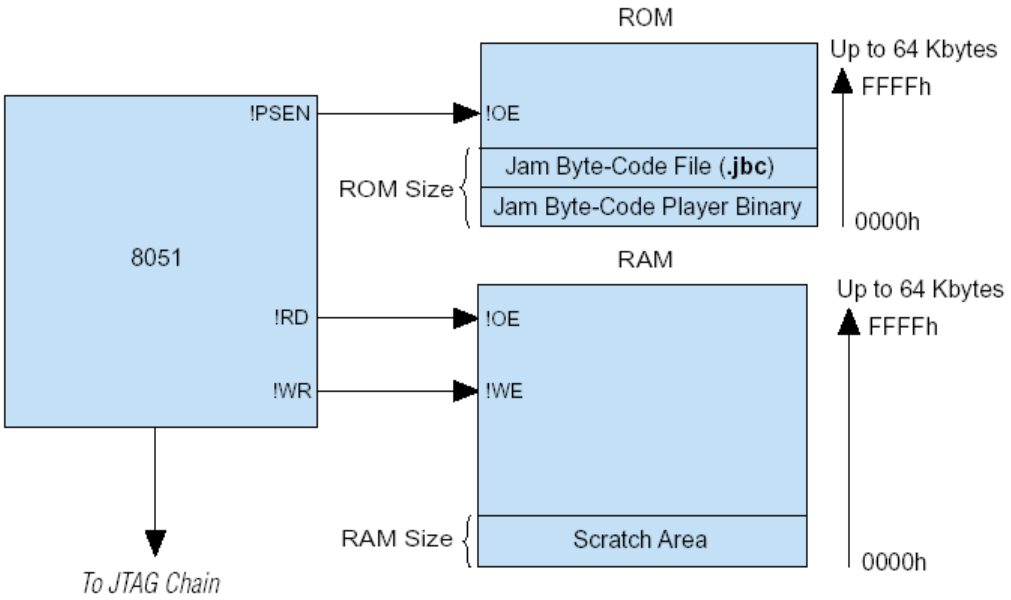
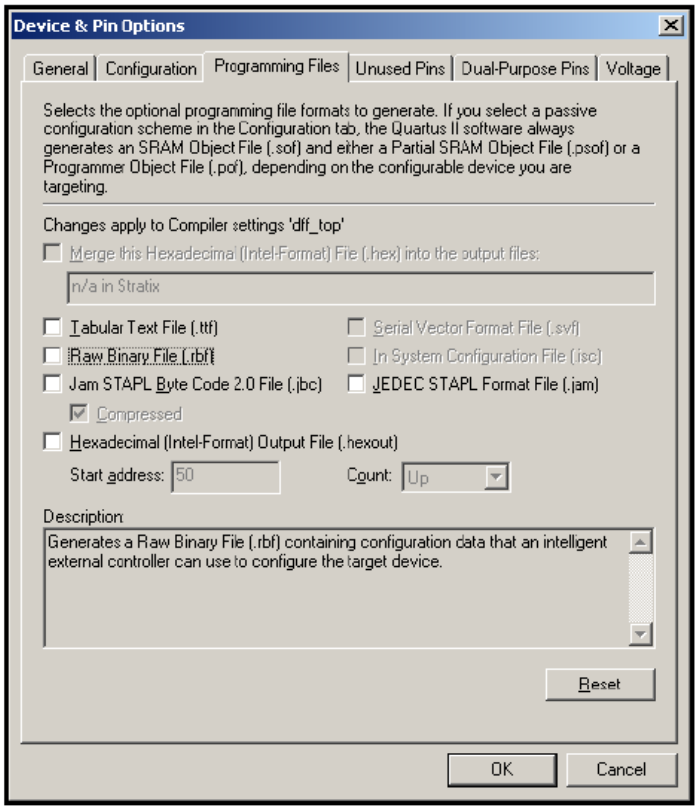


Figure 7–1. Programming Files Dialog Box



Technológia hraničných testov (JTAG)

Figure 1. IEEE Std. 1149.1 Boundary-Scan Testing

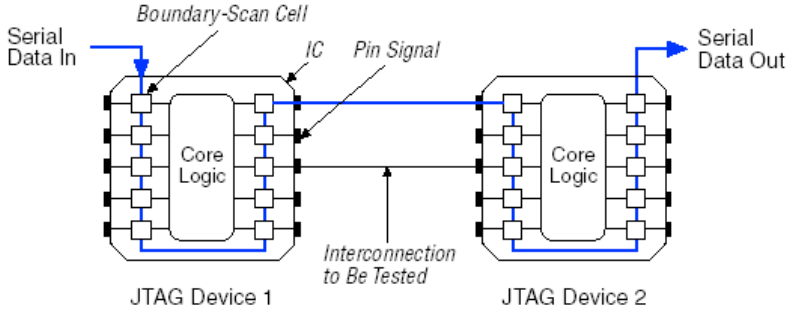


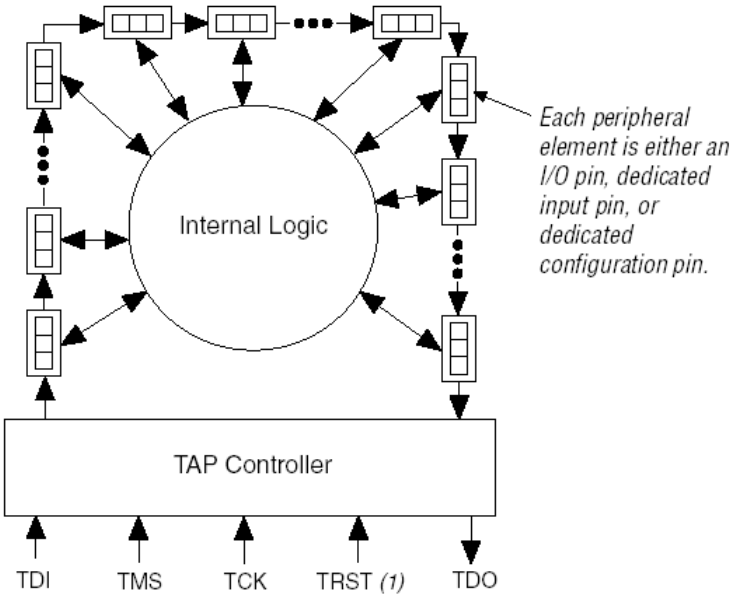
Table 2. IEEE Std. 1149.1 Pin Descriptions

Pin	Description	Function
TDI	Test data input	Serial input pin for instructions as well as test and programming data. Data is shifted in on the rising edge of TCK.
TDO	Test data output	Serial data output pin for instructions as well as test and programming data. Data is shifted out on the falling edge of TCK. The pin is tri-stated if data is not being shifted out of the device.
TMS	Test mode select	Input pin that provides the control signal to determine the transitions of the TAP controller state machine. Transitions within the state machine occur at the rising edge of TCK. Therefore, TMS must be set up before the rising edge of TCK. TMS is evaluated on the rising edge of TCK.
TCK	Test clock input	The clock input to the BST circuitry. Some operations occur at the rising edge, while others occur at the falling edge.
TRST	Test reset input (optional)	Active-low input to asynchronously reset the boundary-scan circuit. (TRST is optional according to IEEE Std. 1149.1). This pin should be driven low when not in boundary scan operation and for non-JTAG users the pin should be permanently tied to GND. It is not supported by all families.

Table 1. Altera Devices with BST Capability

Family	Devices Supporting BST
HardCopy® Stratix®	All devices
Stratix	All devices
Stratix GX	All devices
Cyclone™	All devices
Mercury™	All devices
APEX™ II	All devices
APEX™ 20K, APEX 20KE	All devices
ACEX® 1K	All devices
FLEX® 10K, FLEX 10KE	All devices
FLEX 8000	EPF8282A, EPF8282AV, EPF8636A, EPF8820A, EPF81500A
FLEX 6000	All devices
MAX® 9000 (including MAX 9000A)	All devices
MAX 7000S *(1)*	EPM7128S, EPM7160S, EPM7192S, EPM7256S
MAX 7000A	All devices
MAX 7000B	All devices
MAX 3000A	All devices
Configuration Devices	EPC2, EPC4, EPC8, EPC16

Figure 3. Boundary-Scan Register



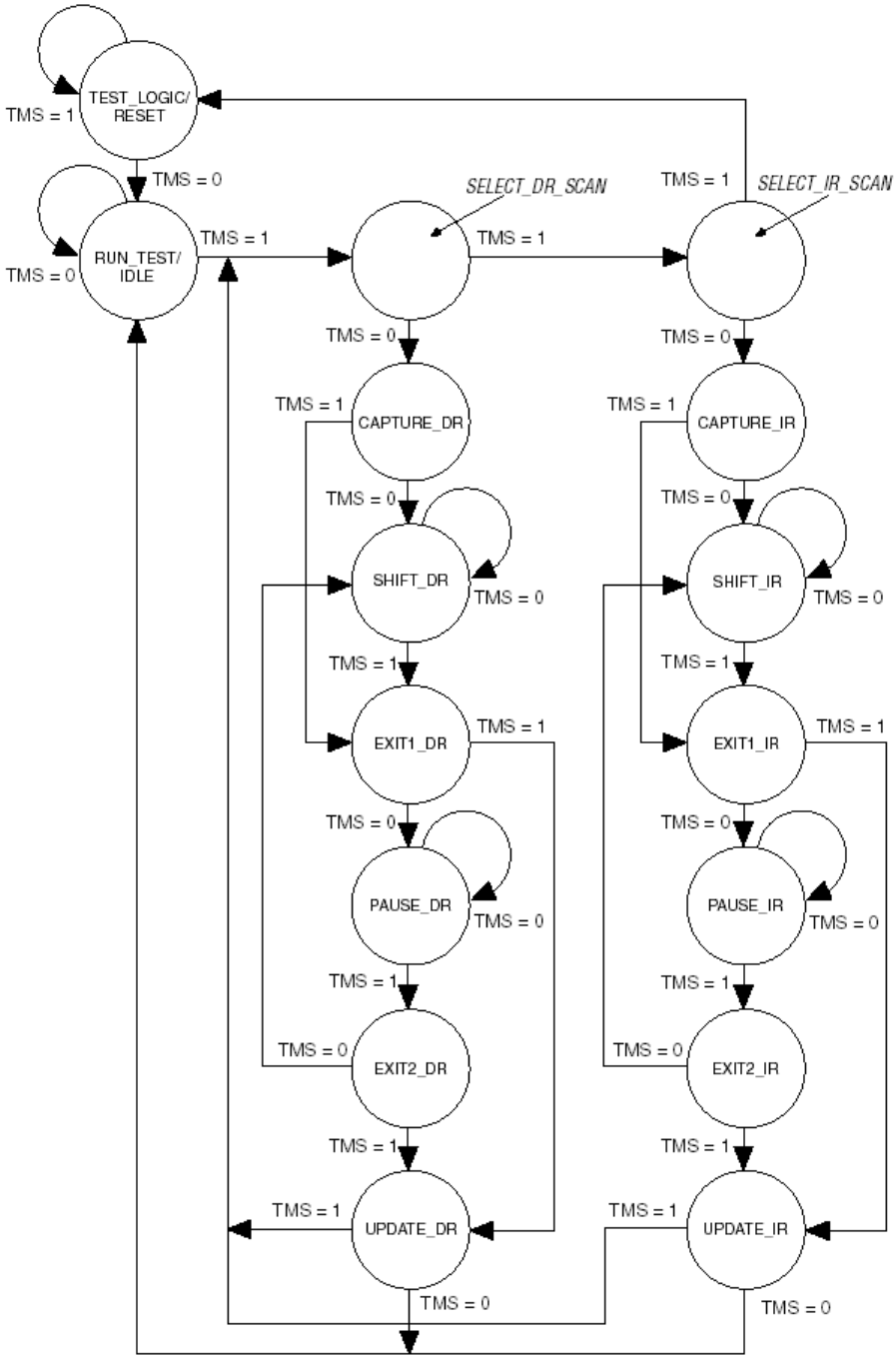
Note to Figure 3:

(1) Refer to the appropriate device family data sheet for TRST pin availability.

Table 11. Boundary Scan Instructions and Descriptions

Mode	Description
SAMPLE/ PRELOAD	Allows a snapshot of the signals at the device pins to be captured and examined during normal device operation, and permits an initial data pattern to be output at the device pins.
EXTEST	Allows the external circuitry and board-level interconnections to be tested by forcing a test pattern at the output pins and capturing test results at the input pins.
BYPASS	Places the 1-bit bypass register between the TDI and TDO pins, which allows the BST data to pass synchronously through the selected device to adjacent devices during normal device operation.
IDCODE	Selects the IDCODE register and places it between TDI and TDO, allowing the IDCODE to be serially shifted out of TDO.
USERCODE	Selects the USERCODE register and places it between TDI and TDO, allowing the USERCODE to be serially shifted out of TDO.
CLAMP *(1)*	Places the 1-bit bypass register between the TDI and TDO pins, which allows the BST data to pass synchronously through selected devices to adjacent devices during normal device operation, while holding I/O pins to a state defined by the data in the boundary scan register.
HIGHZ *(1)*	Places the 1-bit bypass register between the TDI and TDO pins, which allows the BST data to pass synchronously through selected devices to adjacent devices during normal device operation, while tri-stating all of the I/O pins.

Figure 10. IEEE Std. 1149.1 TAP Controller State Machine



Podrobnejší opis JTAG rozhrania
http://cs.felk.cvut.cz/~kubatova/jtag.pdf

Demo čipu s JTAG rozhraním
Dmonštračný výučbový program umožňuje simuláciu jednoduchého čipu s JTAG rozhraním a umožňuje lepšie pochopenie základných princípov tohto rozhrania. Tento program slúži ako doplnkový materiál k prednáške.
http://www.kemt.fei.tuke.sk/Predmety/KEMT412_SPvT/_materialy/Prednasky/6/DEMO/

Byte Blaster II Hardware

Figure 1–1. The ByteBlaster II Download Cable

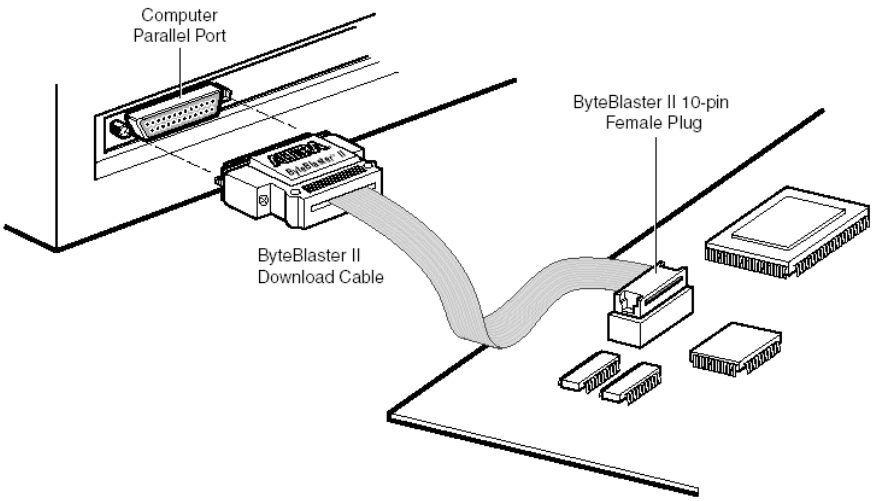


Figure 2–1. ByteBlaster II Block Diagram

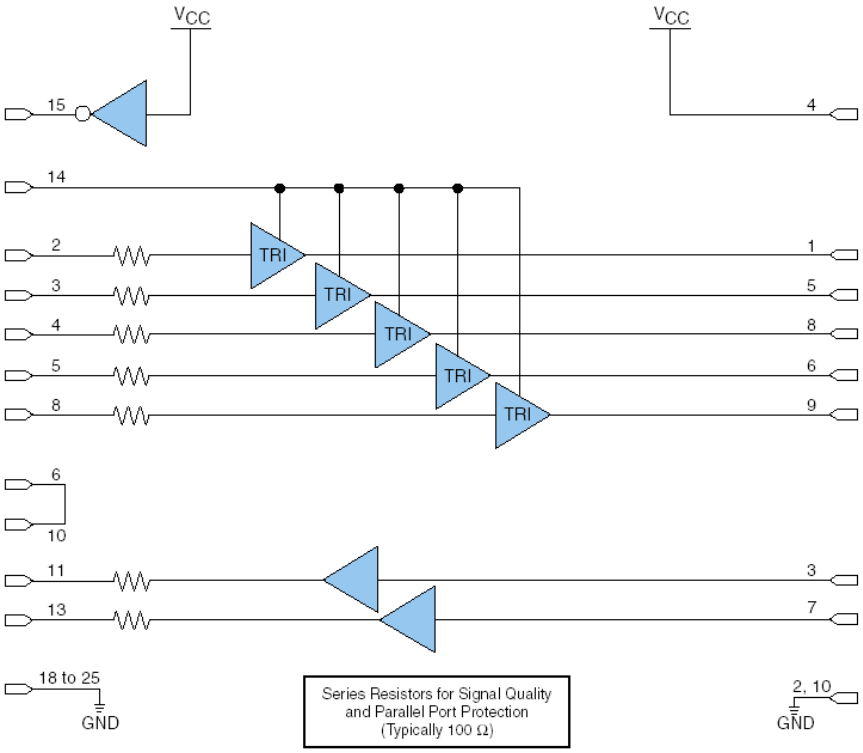
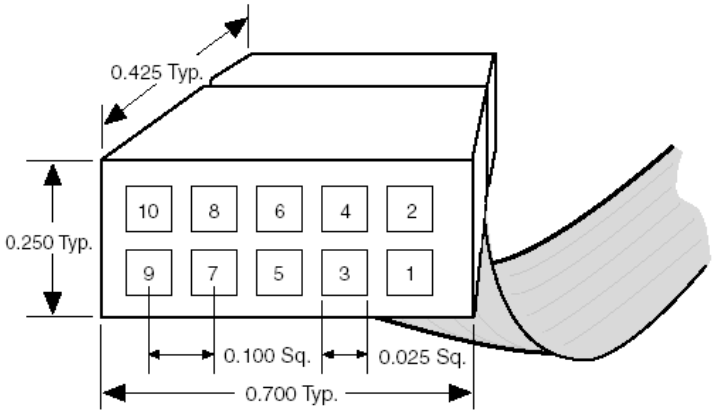


Figure 2–2. ByteBlaster II 10-Pin Female Plug Dimensions



Dimensions are shown in inches. Spacing between pin centers is 0.1 inches.

Table 2–3 identifies the 10-pin female plug signal names and the corresponding programming mode.

Table 2–3. ByteBlaster II Female Plug Signal Names & Programming Modes

Pin	AS Mode		PS Mode		JTAG Mode	
	Signal Name	Description	Signal Name	Description	Signal Name	Description
1	DCLK	Clock signal	DCLK	Clock signal	TCK	Clock signal
2	GND	Signal ground	GND	Signal ground	GND	Signal ground
3	CONF_DONE	Configuration done	CONF_DONE	Configuration done	TDO	Data from device
4	VCC(TRGT)	Target power supply	VCC(TRGT)	Target power supply	VCC(TRGT)	Target power supply
5	nCONFIG	Configuration control	nCONFIG	Configuration control	TMS	JTAG state machine control
6	nCE	Cyclone chip enable	—	No connect	—	No connect
7	DATAOUT	Active serial data out	nSTATUS	Configuration status	—	No connect
8	nCS	Serial configuration device chip select	—	No connect	—	No connect
9	ASDI	Active serial data in	DATA0	Data to device	TDI	Data to device
10	GND	Signal ground	GND	Signal ground	GND	Signal ground

USB Byte Blaster Hardware

Figure 1–1. The USB-Blaster Download Cable

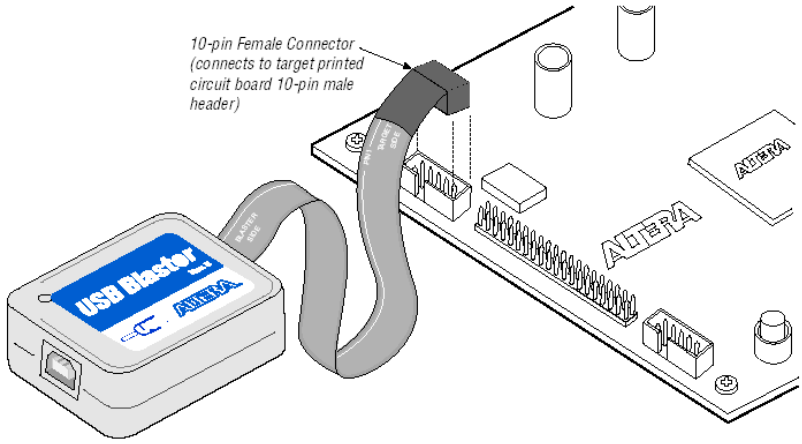
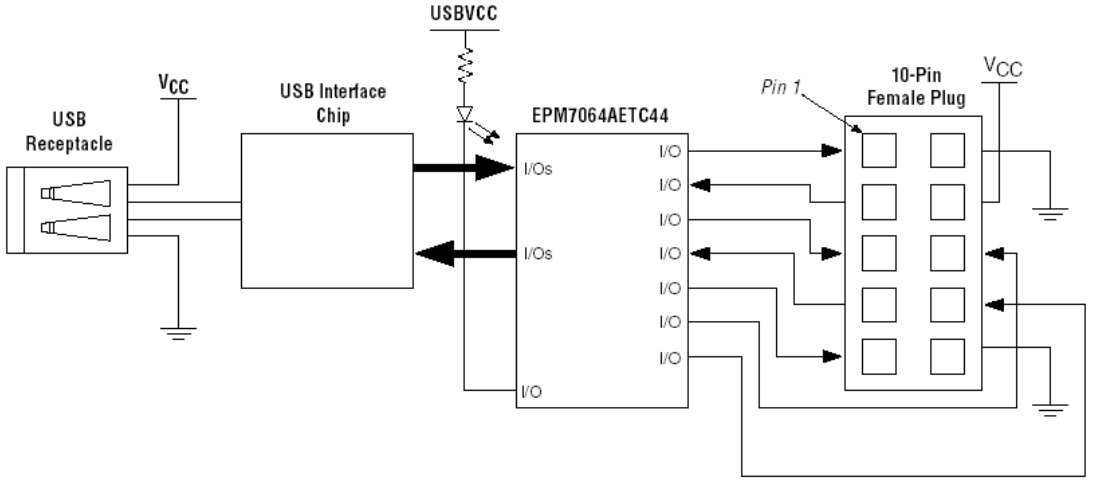


Figure 2–1. USB-Blaster Block Diagram



Signal Tap Embedded Logic Analyzer Megafunction

- Provided with the Quartus II software
- Probes internal nodes while the design is running at system speeds
- Requires no design modification
- Provides non-intrusive probing of ball-grid array (BGA) pins
- Logic analyzer controls available within the Quartus II design software include:
  - Signal selection
  - Trigger setup
  - Memory configuration
  - Waveform display

Základný princíp

Figure 1. SignalTap Logic Analyzer

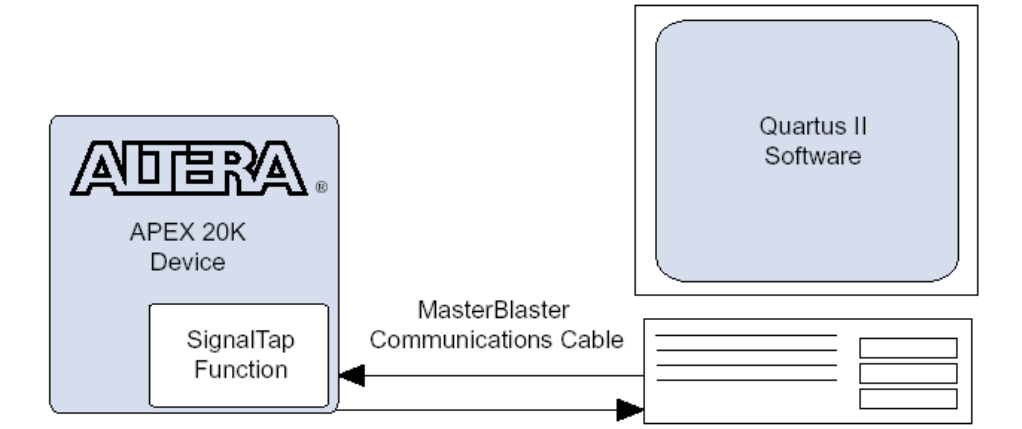


Figure 3. Embedded Logic Analyzer Architecture