RC Extraction

of an Inverter Circuit

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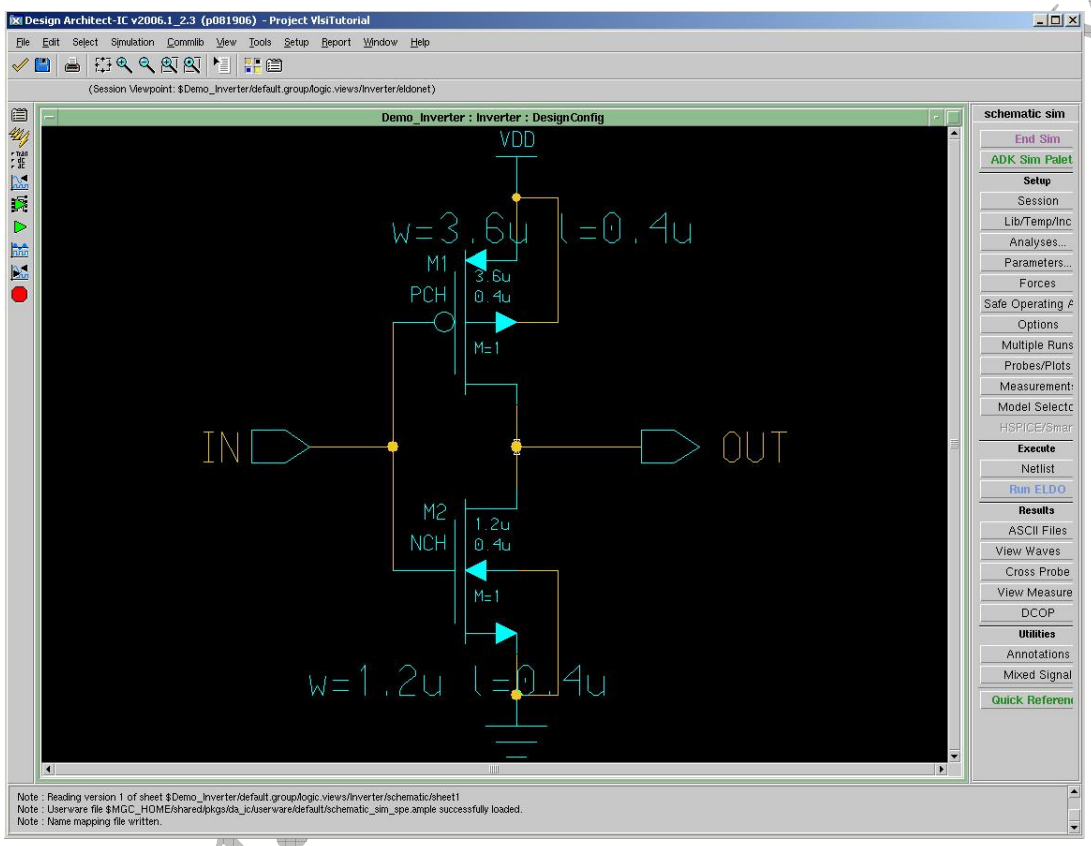
1. Objective

This tutorial shows a step-by-step procedure for parasitic extraction and post-layout simulation of a simple digital inverter cell.

The following schematic was drawn in a previous tutorial:



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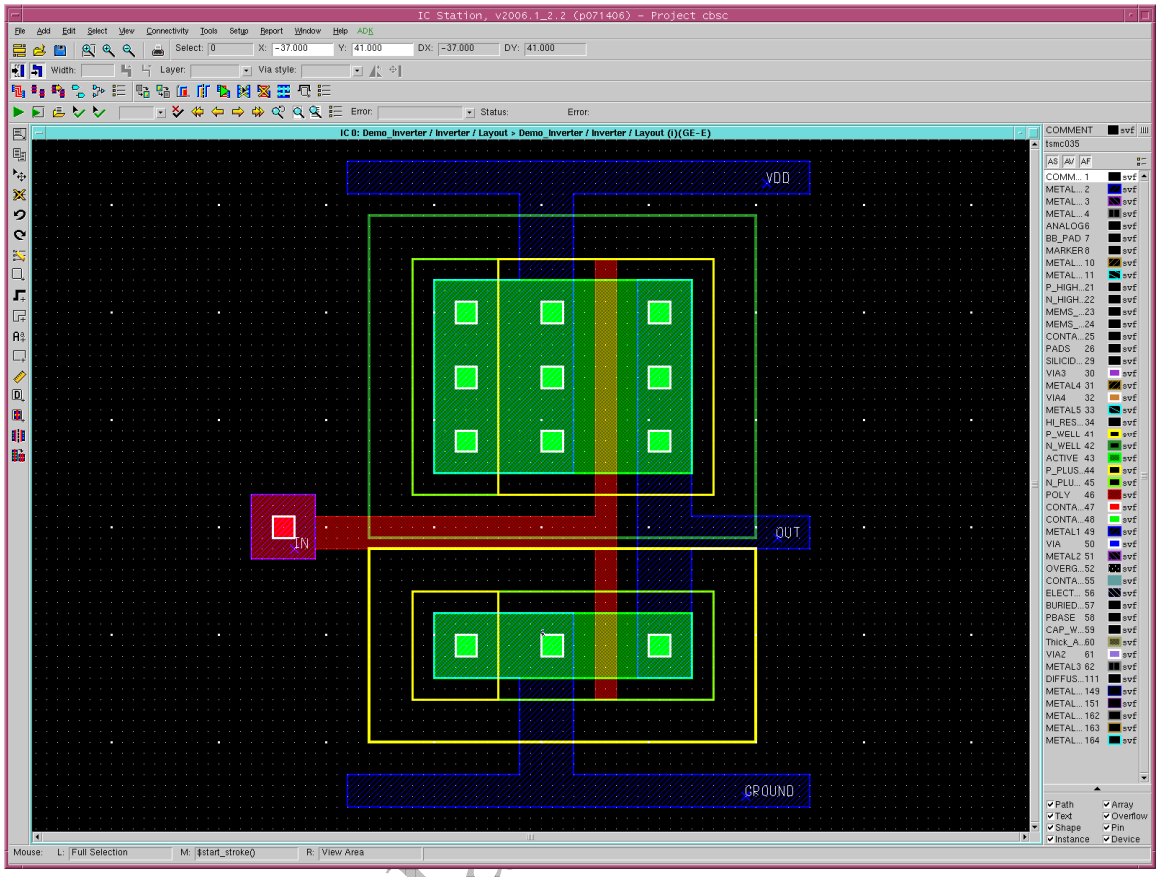
The layout associated with this circuit was drawn in the second tutorial:



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2. Setup & Preparation

The set of directives listed below is applicable to users of the ***Engineering Design Center at Santa Clara University.*** If you are working in a different environment please check with your system administrator.

The steps below are necessary only for the first time to setup the Mentor Graphics environment by changing the settings in your .profile file.
Add the following lines in your **.profile**:

setup mentor-2008.1
alias swd="export MGC_WD=\'pwd\'"

Remember to execute

$. profile

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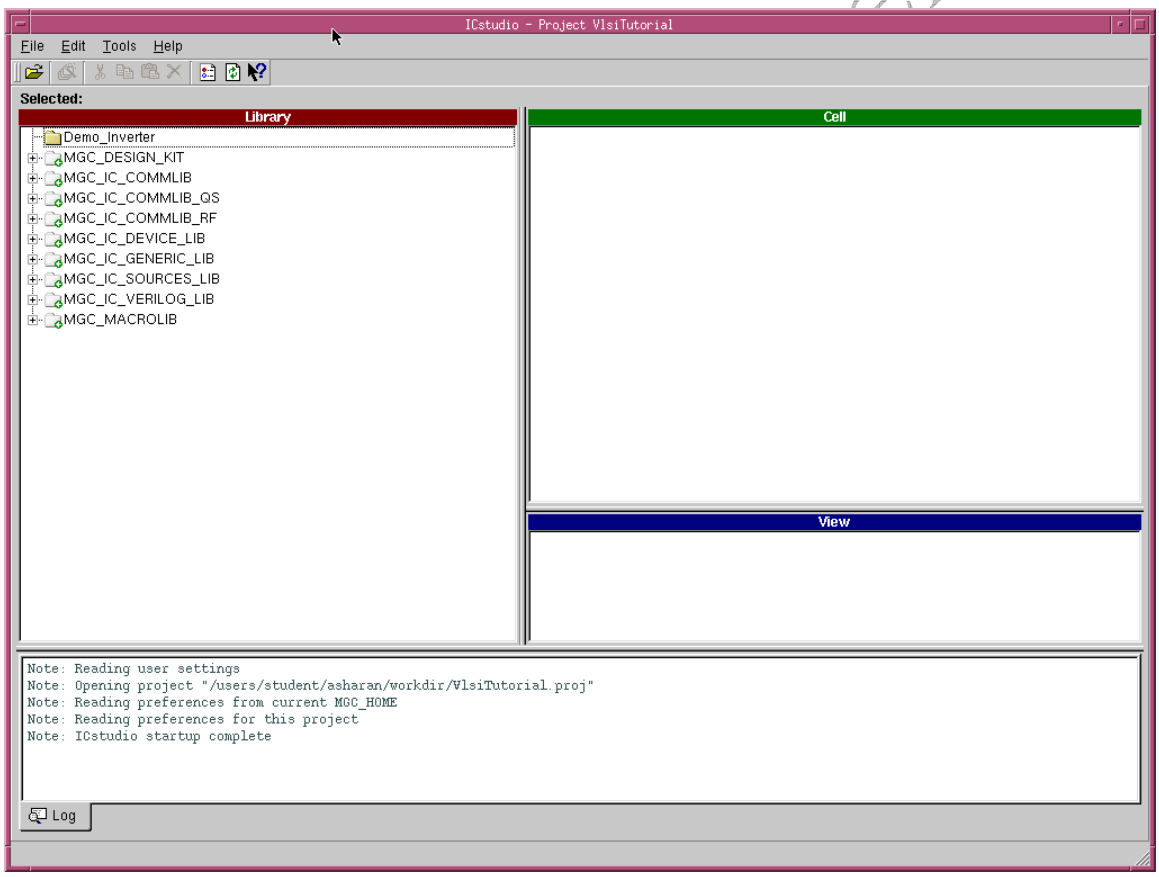
3. Launching IC Studio

On the command line

- To Create a directory to contain your projects type: **"mkdir Tutorial"**
- To change the current directory to Tutorial type: **"cd Tutorial".**
- To open ICSTUDIO type: **"icstudio".**

This launches the ICStudio window shown below.



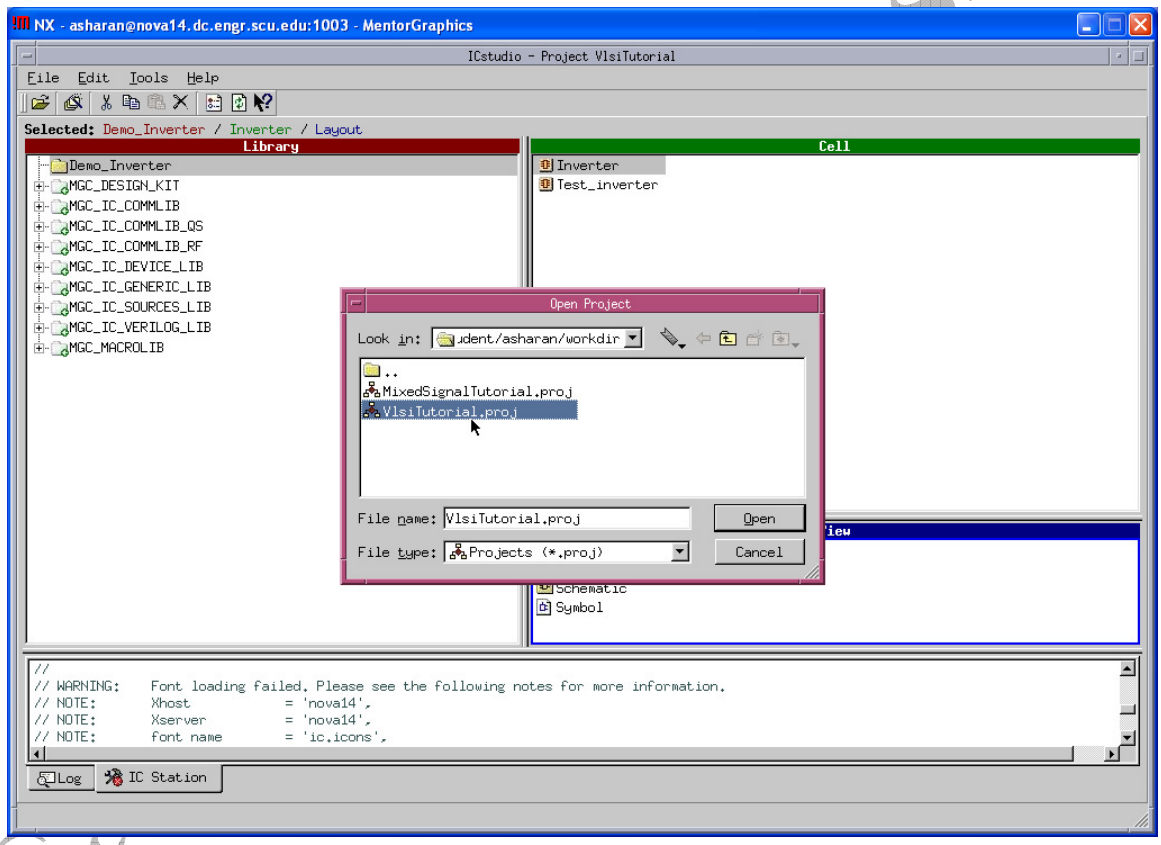
4. Opening the Project

To create a project the follow the three steps given below:

1. Opening icstudio and opening the project

On the ICStudio Window

- Click **File -> Open -> Project** to create a new project.
- Enter the **Project name** (e.g vlsi_tutorial) and the **Project Location**
- Click **Open** in the **Open Project** pop-up window
- When the project opens, double-click on the **Layout** view to launch ICStudio and view your circuit layout.



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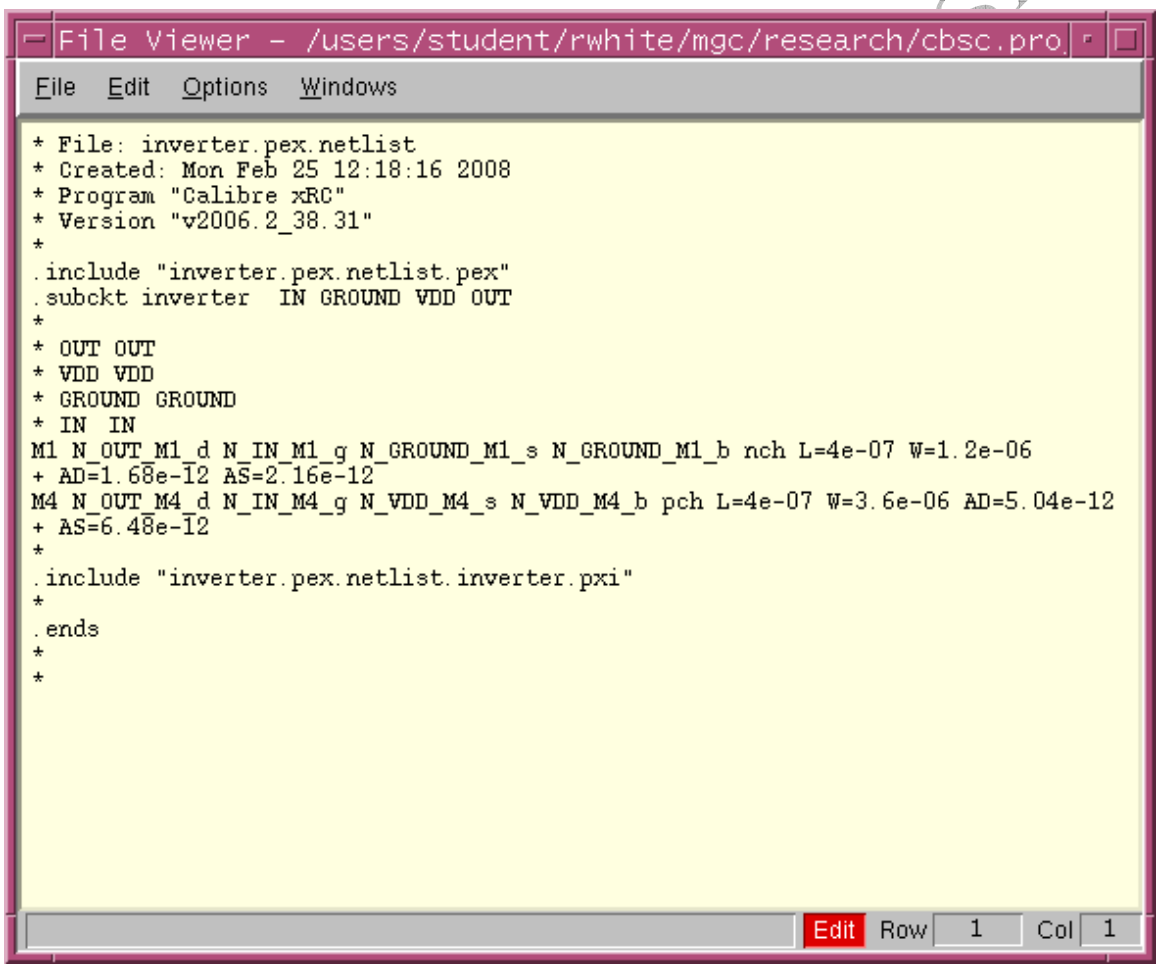
5. Parasitic Extraction

After completing the DRC and LVS checks, we can proceed to extract parasitic capacitances and resistances of the actual layout.

- Click **Tools > Run PEX**
- Check the box **Export from Schematic Viewer** under **Inputs**
- Click **Run PEX**

The extraction should run, producing a PEX netlist like the one below:

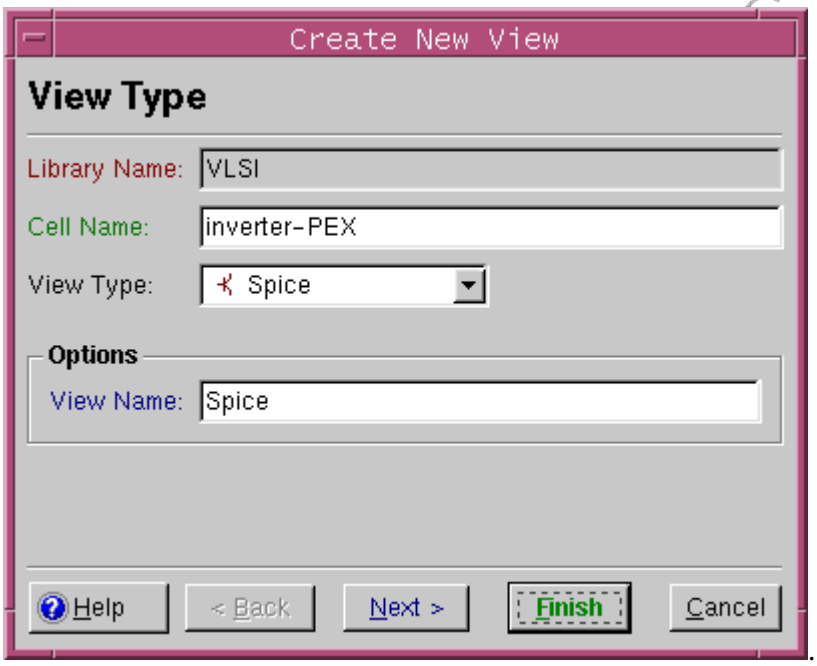


6. Post-Layout Simulation

After successful layout and verification, we would like to re-simulate our circuit including all of the parasitic capacitances and resistances generated by the PEX tool. We will import the generated PEX netlist back into ICStudio as a SPICE file.

On the ICStudio Window

- Click **File -> New -> View** and select **Spice** as the view type
- Enter a name such as Inverter-PEX, and click **Finish**

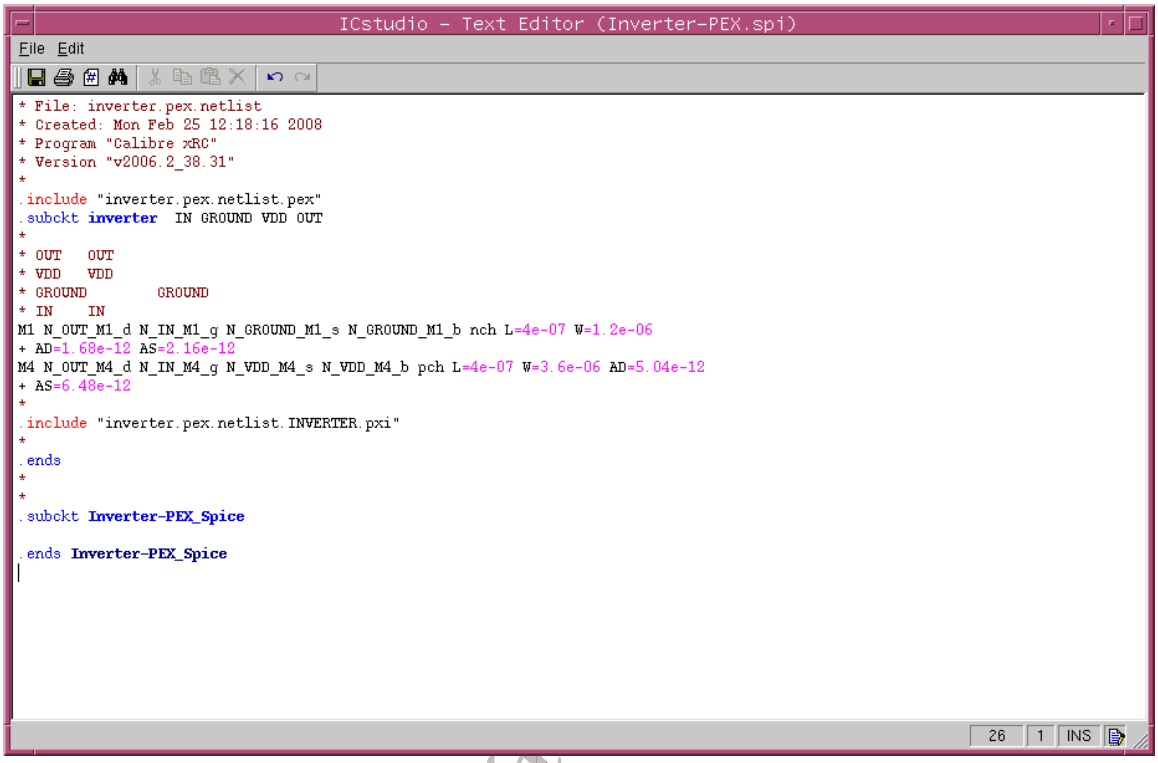


- From the menu, select **File > Insert File**
- Go to the calibre directory of your current project: This path will typically be something like:

~/mgc/VLSItutorial.proj/Inverter.lib/default.group/layout.views/inverter/inverter.cal/

- Select the file: “inverter.pex.netlist”

The Netlist should appear as shown below:



We need to make a few changes to complete a proper Spice Netlist:

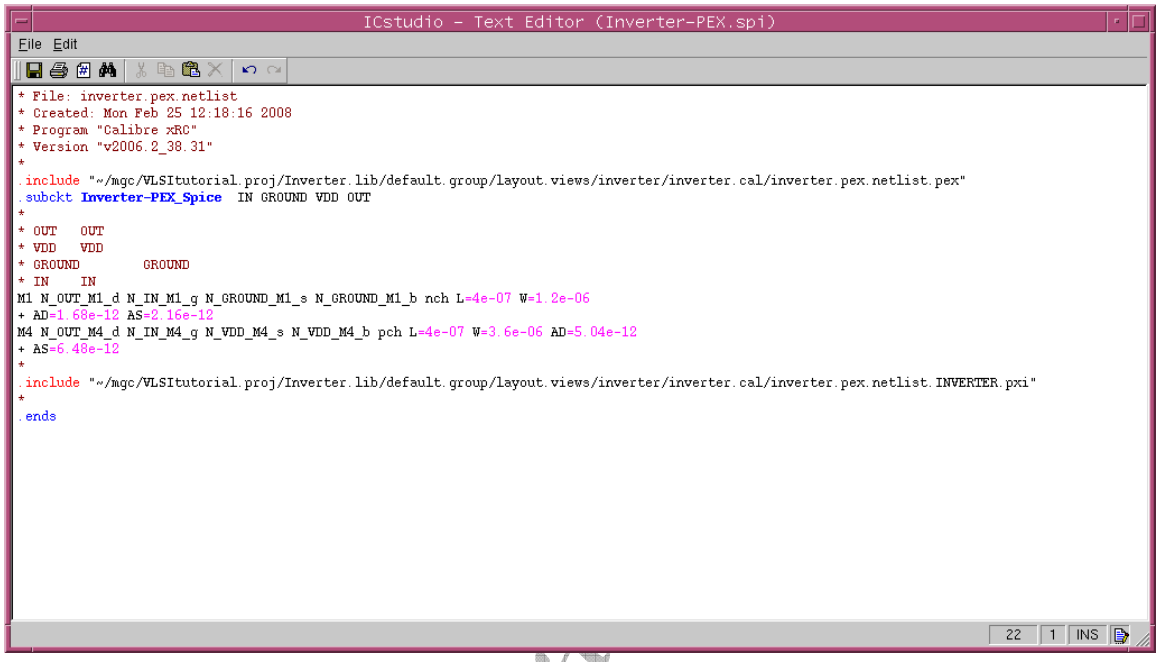
- First, delete the last two lines of the file :
  (.subckt Inverter-PEX_Spice & .ends Inverter-PEX_Spice)
- Now, at the top of the netlist, where the subcircuit name is given as “inverter”, change “inverter” to Inverter-PEX_Spice
- The next change is to enter the full paths for the two **.include** statements:
  Change the following lines to reflect your actual path:

  .include "inverter.pex.netlist.pex"
  .include "inverter.pex.netlist.INVERTER.pxi"

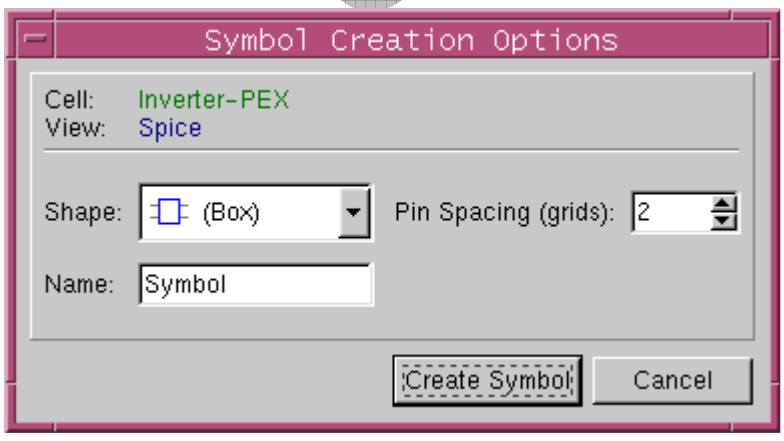
These lines should change to :
.include
"~/mgc/VLSItutorial.proj/Inverter.lib/default.group/layout.views/inverter/inverter.cal/inverter.pex.netlist.pex"
.include
"~/mgc/VLSItutorial.proj/Inverter.lib/default.group/layout.views/inverter/inverter.cal/inverter.pex.netlist.INVERTER.pxi"

Note: Please use your actual path – the above changes will probably be different for your path.

The completed netlist looks like this:

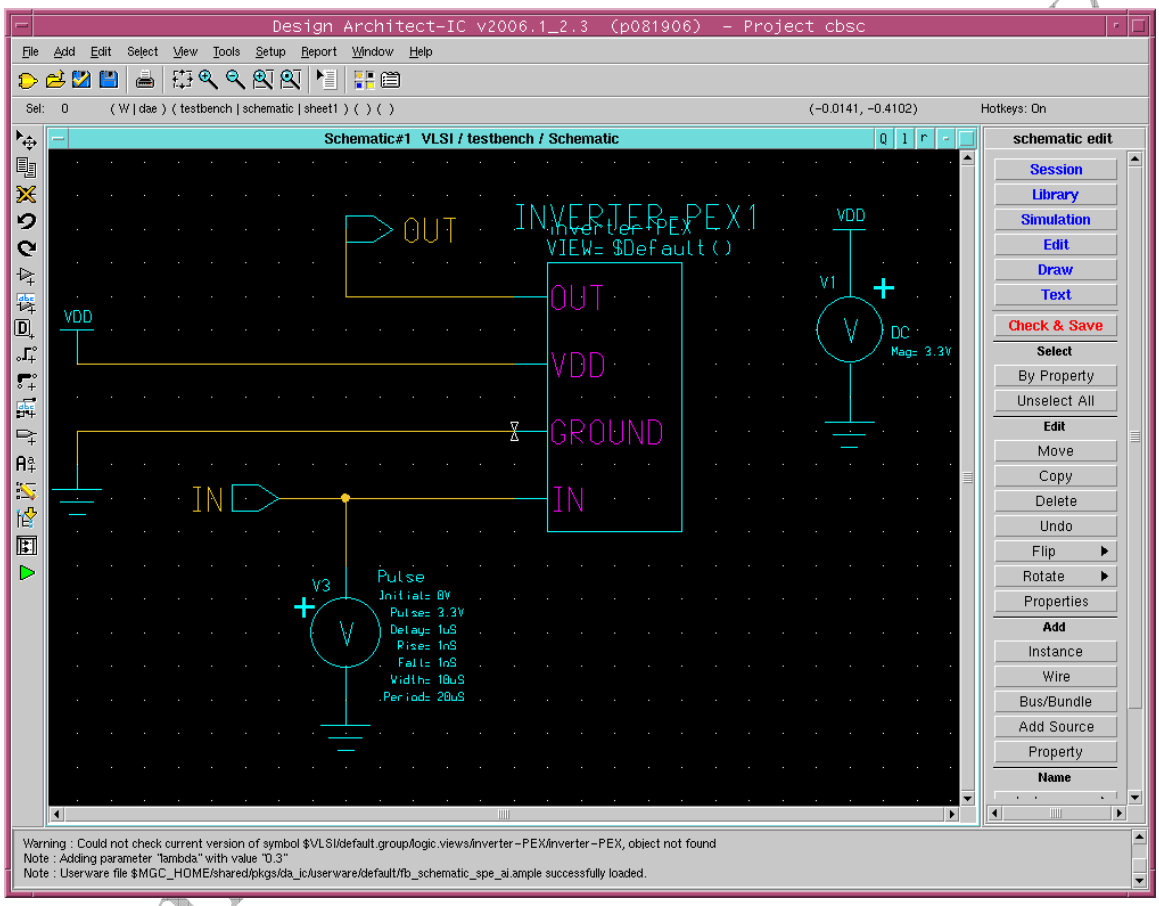


- Save the file and close it.
- After closing the file, a box will pop up to generate a symbol.
- Click **Create Symbol**



7. Running the Simulation

- From ICstudio, create a new schematic view, and instantiate the Inverter-PEX cell.
- Add a VDD DC supply voltage source and a PULSE voltage source for the input.
- Enter simulation mode and Run the simulation



- Plot the resulting data with EZWave to see the performance of the circuit including parasitics: