DoCD™

DCD on Chip Debug System

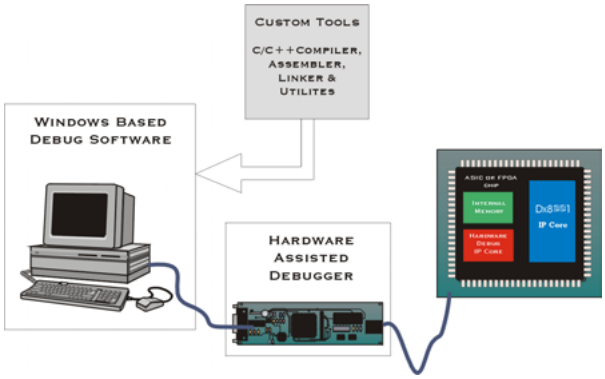
ver 1.16

OVERVIEW

The most important possibility for SoC designers are pre-silicon debugging. DCD has introduced into the market a new 8051 and 80390 IP Cores family with an embedded Debug IP Core. DCD on Chip Debug System (DoCD™) prominently cuts debugging time. Integrating DCD IP Cores with a Hardware Assisted Debugger and Debug IP Core provides a powerful SoC development tool with advanced features.

The DoCD™ system consists of three major blocks:

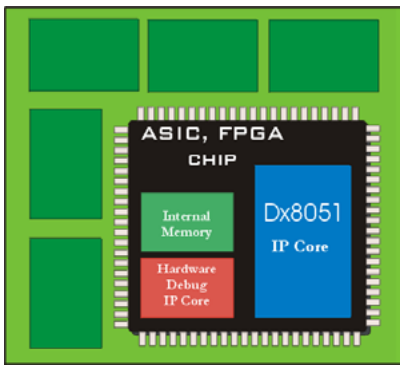
- Debug IP Core
- Hardware Assisted Debugger
- Debug Software



The Debug IP Core block provides an in-circuit emulator feature. A high-performance Hardware Assisted Debugger is connected to the target system containing the DCD's core either in FPGA or ASIC. The Hardware Assisted Debugger manages communication between the Debug IP Core inside silicon and Debug Software.

Debug IP Core

The Debug IP Core can be provided as VHDL or Verilog source code as well as CPLD/FPGA EDIF netlist depending on the customer requirements. Because many SoC designs have both power and area limitations, DoCD™ provides a scaled solution. Debug IP Core can be scaled to control gate count. The benefit is fewer gates for lower power and core size while trading off debug capability. Typically, all of the features are utilized in pre-silicon debug (i.e. hardware emulation or FPGA evaluation) with a lesser feature set shipped in final silicon.



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KEY FEATURES OF DEBUG IP CORE

- Processor execution control
  - *Run, Halt*
  - *Reset*
  - *Step into instruction*
  - *Skip Instruction*
- Read-write all processor contents
  - *Program Counter (PC)*
  - *Program Memory*
  - *Internal (direct) Data Memory*
  - *Special Function Registers (SFRs)*
  - *External Data Memory*
- Unlimited number of software breakpoints
  - *Program Memory*
  - *Internal (direct) Data Memory*
  - *Special Function Registers (SFRs)*
  - *External Data Memory*
- Hardware execution breakpoints
  - *Program Memory*
  - *Internal (direct) Data Memory*
  - *Special Function Registers (SFRs)*
  - *External Data Memory*
- Hardware breakpoints activated at a
  - *certain program address (PC)*
  - *certain address by any write into memory*
  - *certain address by any read from memory*
  - *certain address by write into memory a required data*
  - *certain address by read from memory a required data*
- Automatic adjustment of debug data transfer speed rate between HAD and Silicon
- Three-wire communication interface
- Fully static synchronous design with no internal tri-states

HARDWARE ASSISTED DEBUGGER

Hardware Assisted Debugger (HAD) is a small hardware adapter that manages communication between the Debug IP Core inside silicon and a serial port of the host PC running DoCD™ Debug Software.

KEY FEATURES OF HAD PCB BOARD

- RS-232 communication interface to target host at 57 600 BPS
- Three wire synchronous communication interface to Debug IP Core
- Supports three I/O voltage standards
  - *5.0 Volt systems*
  - *3.3 Volt systems*
  - *2.5 Volt systems*
- Single power supply directly from target board within 2.9 V to 5 V
- Low current consumption within 40-60 mA
- Small physical dimensions

DEBUG SOFTWARE

The DoCD™ Software (DS) is a Windows® based application. It is fully compatible with nearly all existing 8051/80390 C compilers and Assemblers. The DS allows user to work in two major modes: software simulator mode and hardware emulator mode. Those two modes assure possibility to pre-silicon software validation in simulation mode and then real-time debugging of developed software inside silicon – using emulator mode. Once loaded, the program may be observed in Source Window, run at full-speed, single stepped by machine or C-level instructions, or stopped at any of the breakpoints.

The DoCD™ Debug Software supports all DCD's 8051/80390 (DR8051x, DR80390x, DP8051x, DP80390x) in the following architectures:

- High Performance RISC – (DR -2 cycle)
- Pipelined High Performance RISC – (DP -1 cycle)

with their particular configurations.

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KEY FEATURES OF DEBUG SOFTWARE

- Two working modes
  - *hardware emulator*
  - *software simulator*
- Source Level Debugging:
  - *C level hardware/software breakpoints*
  - *C code execution*
    - *line by line*
    - *over line*
    - *out of function*
    - *skip line*
  - *ASM code execution*
    - *Instruction by instruction*
    - *over instruction*
    - *out of function*
    - *skip instruction*
  - *ASM, C source view of code*
- Symbol Explorer provides hierarchical tree view of all symbols:
  - *modules*
  - *functions*
  - *blocks*
  - *variables and more*
- Contents sensitive Watch window
- Symbolic debug including:
  - *code*
  - *variables*
  - *variable types*
- Unlimited number of software breakpoints
  - *Program Memory*
  - *Internal (direct) Data Memory (IDM)*
  - *Special Function Registers (SFR)*
  - *eXternal Data Memory (XDM)*
- Real-time hardware breakpoints
  - *Program Memory*
  - *Internal (direct) Data Memory (IDM)*
  - *Special Function Registers (SFR)*
  - *eXternal Data Memory (XDM)*
- Set/clear software or hardware breakpoints in Disassembled and C Source Code windows
- 1024 steps deep Software Trace
- Load Program Memory content from:
  - *OMF-51, extended OMF-51 files*
  - *OMF-251 file*
  - *Intel HEX-51, HEX-386 files*
  - *BIN file*
- Auto refresh of all windows during execution of program
  - *Registers' panel including ACC, B, PSW, PC, SP, DPTR, DPP and four banks of general purpose registers R0-R7*
  - *Internal (direct) Data Memory (IDM)*
  - *Special Function Registers (SFR)*
  - *eXternal Data Memory (XDM)*
  - *Timers/Counters*
  - *UARTs*
  - *I/O Ports*
- Dedicated windows for peripherals
- Configurable auto refresh time period with 1s step resolution
- Status bar containing number of actually executed instructions, number of clock periods and real processor speed rate
- Three wire communication Hardware Assisted Debugger interface
- The system runs on a Windows® 95/98/NT/2000/XP PC
- Supports software tools from Keil, Archimedes, IAR, Tasking, Franklin, SDCC and the others

SPECIAL FEATURES OF DEBUG SOFTWARE

- Load Program Memory content from:
  - *NOI files*
  - *IEEE 695 files*
- Command line:
  - *command history*
  - *scripts execution*
- Call stack tracing
- Real-time Hardware Trace
- User defined variables

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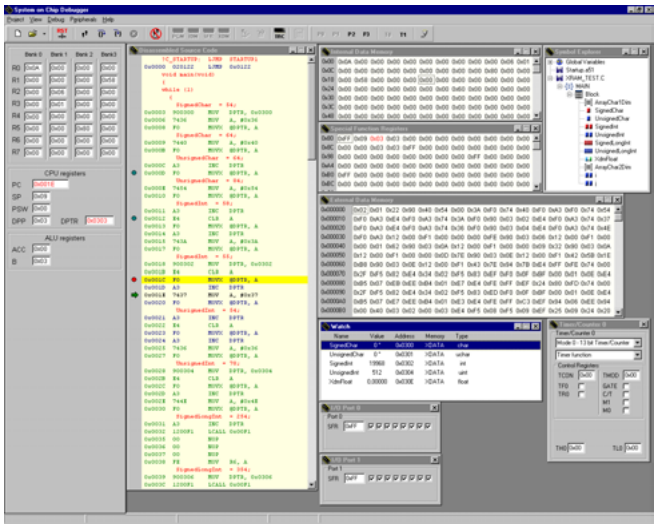

DEBUG IP CORE PINOUT

The following pins are used by DoCD™ debug IP Core.

PIN	TYPE	DESCRIPTION
docddatai	input	DoCD™ data input
docddatao	output	DoCD™ data output
docdclk	output	DoCD™ clock line

AREA UTILIZATION

The following table give a survey about the Debug IP Core area in the FPGA and ASIC devices.

Device vendor	Area
ALTERA	720 LC
XILINX	360 Slices
ASIC	2500 gates

SYSTEM FEATURES

- ### SOFTWARE BREAKPOINTS:

  An unlimited number of software breakpoints can be set anywhere in the physical address space of the processor. This means that breakpoints can be set in Program Memory space, direct RAM, SFRs and external RAM. If at least one software breakpoint is set program is executed in automatic step by step mode, with checking if certain breakpoint condition is met. Program execution is halted when breakpoint condition is already met, and its execution can be resumed at any time in any appropriate mode.

- ### HARDWARE BREAKPOINTS:

  The number of hardware breakpoints is limited to four in different address spaces. Like software breakpoints, hardware execution breakpoints can be set in Program Memory space, direct RAM, SFRs and external RAM. Like their software counterparts, they stop program execution just prior to an instruction being executed. The difference is found in the method of program execution. In this case program is run with full clock speed (in real-time), and processor is halted when hardware signalizes true breakpoint condition.

- ### MIXED MODE BREAKPOINTS:

  Mixed breakpoint mode is also allowed and it means that software and hardware breakpoints are mixed in the system. This gives user a flexibility in the debugging. For example two different break conditions can be set at the same address space using software and hardware breakpoints. In each breakpoint mode halt means: CPU is halted and instructions are no longer being fetched, all peripherals running and are not affected by halt.

- ### SYMBOL EXPLORER:

  Symbol Explorer provides hierarchical tree view of all C project symbols. It supports all C types, variables, constants, functions, and symbolic names of registers. Along with watch window provides flexible and powerful debugging feature at high C language level.

- ### SCALED SOLUTION:

  Because many SoC designs have both power and gate limitations, DCD provides a scaled solution. Debug extensions can be scaled to control gate counts. The benefits are fewer gates, lower power and core size while trading off debug capability.

- ### HOST REQUIREMENTS:

  A Pentium class computer with minimum 32 MB of memory, 10 MB of free space on Hard Disk, CD-ROM drive, RS232 serial port, and Windows® 98/Me or Windows® NT/2000/XP operating system are required.

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