

Actel Fusion™

THE WORLD'S ONLY SINGLE-CHIP SYSTEM MANAGER



System Management continues to gain importance in the design of all electronic systems. Smaller process geometries drive more multi-volt devices and are more susceptible to voltage and temperature fluctuations. While system management designs can run into hundreds of discrete components, the Actel Fusion Programmable System Chip (PSC), the industry's only mixed-signal field-programmable gate array (FPGA) solution, can integrate these system management functions and provide programmable flexibility and system-level integration—all in a single chip. Unprecedented integration in Fusion devices can offer cost and space savings of 50% or greater relative to current implementations.

Actel, the world's only supplier of mixed-signal FPGAs, now offers the only single-chip system management solution. The Actel Fusion PSC integrates configurable analog, large Flash memory blocks, comprehensive clock generation and management circuitry, and high performance programmable logic in a monolithic device. Actel has developed turn-key solutions, including a development kit and a software GUI for system management. This level of integration, configurability, and support establishes Fusion as the definitive system management solution.

System Management Key Tasks

- Power Management
 - Up to 10 Power Supplies, -11 V to +12 V
 - Power-On Detection and Reset
 - Power-Up Sequencing
 - Voltage Monitoring
 - Current Monitoring
- Thermal Management
 - Track and Control Up to 10 Remote Sensors
- System Clocking
 - Backup System Clock
- SRAM FPGA Management
- Boot Loader for MCU
- Remote Communications
- Error/Alarm Recovery
- Diagnostics/Prognostics
- Identification/Authentication
- Low Power Operation

Actel Fusion PSC: The Comprehensive Single-Chip System

System Management Trends and Challenges

System management is a collection of seemingly unrelated tasks with the goal of ensuring the proper operation of the system. These tasks focus on maximizing system uptime, identifying and communicating alert conditions, and logging data and alarm conditions. Boards must also be able to initiate corrective action when fault conditions occur.

Driven by the need to increase system uptime and reliability, many systems are adding in-system diagnostics and prognostics, not only to help debug systems that have failed but also to identify potential failures before they arise. In standards-driven markets, reliability and uptime are key metrics by which OEMs can differentiate themselves.

System Management Functions

	Power-On	Power-Up	System Operational	Power-Down
Power Initialization	✓			
Power Sequencing		✓		✓
Reset Management	✓			
Voltage Monitoring	✓	✓	✓	✓
System Clocking	✓	✓	✓	✓
Data Logging	✓	✓	✓	✓
Remote Communications	✓	✓	✓	✓
Diagnostics and Prognostics	✓	✓	✓	✓
Errors and Alarms	✓	✓	✓	✓
Current Monitoring		✓	✓	
SRAM FPGA Management		✓	✓	✓
Thermal Management			✓	
MCU Boot Loader			✓	
ID and Authentication			✓	

Today's Solution

Current system management implementations require a large number of discrete components (sometimes numbering in the hundreds), occupy large amounts of board space, and are inflexible to change. These solutions are a collection of fixed function chips and discrete components that must work in concert to create a cohesive solution: CPLD, real-time clock, power sequencer, temperature monitor, fan controller, nonvolatile memory, PWM, configuration memory, etc. In addition to consuming board space, the large number of components adds to cost both directly (unit cost, assembly cost, inventory cost) and indirectly (design time, procurement, discontinuation). Increased

component count also contributes directly to the failure rate: eliminated parts will not fail! These hardware-implemented discrete solutions often require board respins even for incremental design changes, making it impossible to create platform solutions and realize higher economies of scale.

Most system management implementations are proprietary, evolving over time within an organization, although standards are being developed and adopted (ATCA, MicroTCA, and IPMI). Today's smaller process geometries running at lower voltages are more sensitive to changes in the board environment, making system management an increasingly important part of any system design.

Management Solution

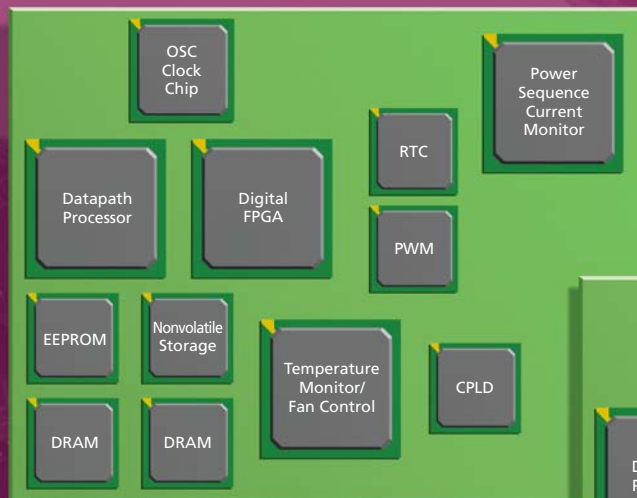


System Management in a Single Chip

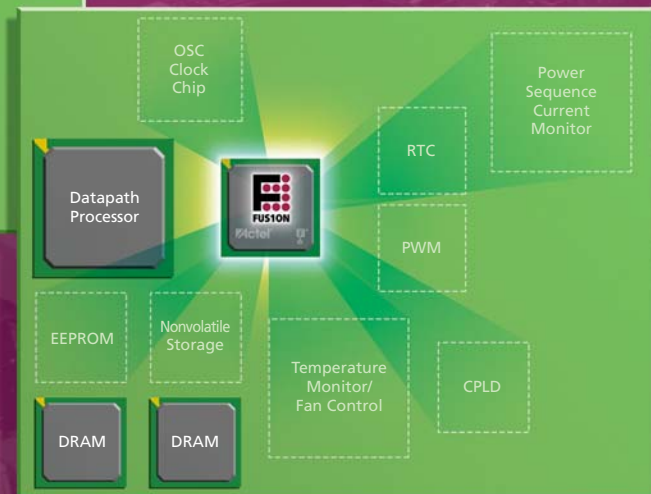
As the world's first mixed-signal FPGA family, Fusion integrates mixed-signal analog, Flash memory, and FPGA fabric in a monolithic PSC. The Actel Fusion devices enable designers to quickly move from concept to completed design and deliver feature-rich systems to market. This new technology takes advantage of the unique properties of Actel Flash-based FPGAs, including a high-isolation, triple-well process, and the ability to support high-voltage transistors to meet the demanding requirements of mixed-signal system design.

Fusion sets the standard in system management as the market's only single-chip solution. Leveraging a unique combination of Flash memory, configurable analog, and Flash FPGA logic, Fusion reduces cost, board space, and design time.

The Fusion device's flexibility enables users to implement proprietary or standards-based system management solutions. As a single-chip implementation, Fusion simplifies design implementation, enabling all system management functions to be configured in a single design environment with superior reliability.



Typical Board Using Current System Management Solution

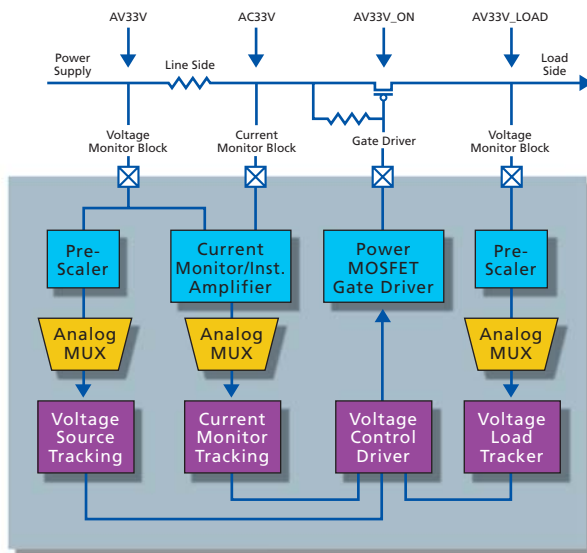


Typical Board Using Fusion System Management Solution

Power Management

Considered the most critical element of system management, Fusion takes aim at power management with an I/O structure specifically designed to effectively and efficiently manage multiple power rails directly. Fusion can manage up to 10 power supplies and connect directly to power rails from -11 V to 12 V without any external components. The Fusion Analog Quad I/O structure combines three analog inputs with a gate driver output. Each analog I/O is individually configurable and can operate independently. Additionally, these I/Os are grouped together to work in concert to support power management. The robust functionality of the Analog Quad allows for the following:

- Power-on detection and reset
- Power-up sequencing and tracking
- Voltage monitoring and trimming
- Current monitoring



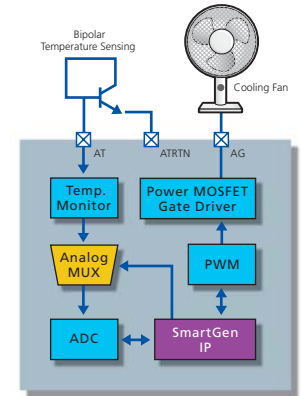
Voltage Rail Control

Fusion can monitor the various power rails, keeping them gated from the rest of the system until they have stabilized. The programmable gate driver can then turn on the power rails in the appropriate sequence and ramp-rate. Load and supply side voltages as well as current consumption can be monitored during operation. Fusion vastly reduces the number of external components required to monitor and sequence power supplies, reducing board space, component count, and cost.

Thermal Management

Maintaining the proper environmental operating conditions is a key component in system management. Today's intelligent systems not only monitor and manage thermal conditions, but also distribute system traffic to better balance the system and maximize performance.

Fusion integrates temperature monitoring capabilities into the Analog Quad, requiring only an external transistor. Fusion supports up to 10 external transistors, enabling designers to track the temperature of many off-chip locations. It is advantageous to track temperatures at various points on the board, including high-end processors and FPGAs.



Fusion Thermal Management

In addition to temperature monitoring, Fusion can handle the fan control to enable closed loop thermal management. Fusion integrated thermal management enables designers to maintain optimal system conditions, leading to increased uptime and performance with fewer components and reduced cost.

SRAM FPGA Management

A drawback to SRAM FPGAs is the hand-holding required to keep them operational. At power-on, volatile SRAM devices must be configured with their respective designs. Fusion integrated Flash memory can store the design files for many different types of FPGAs, eliminating a separate configuration PROM from the board. As volatile devices, SRAM FPGAs are very concerned with supply voltage "brownouts," which are dips in supply voltage that place the device in an unknown state. These voltage rails must be monitored closely for any variance (dips as small as 60 mV) that would require an FPGA reset.

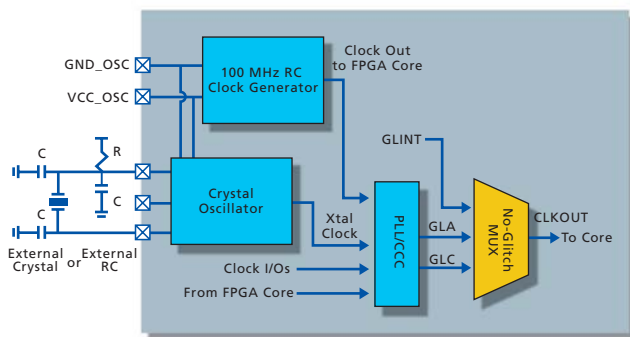
The unique Fusion feature set makes it an ideal SRAM FPGA management device, eliminating boot PROMs and brownout detection devices, sequencing the power-up, and further reducing board space and overall cost.

System Clocking

Proper clock generation and distribution is critical to system operation. Whether the clock source is external to the system or internally generated, the robust Fusion clock distribution and generation resources are up to the task.

Fusion devices support both internal and external clock sources, including an integrated 100 MHz RC oscillator that requires no components. The 100 MHz RC oscillator is accurate to 3% over the industrial temperature range. For systems that require higher precision, an external crystal can be connected to the Fusion crystal oscillator circuit.

Integrated clock conditioning circuits (CCCs) and phase-locked loops (PLLs), combined with high-speed, low-skew networks, allow for the manipulation and distribution of very accurate clock sources to both on-chip and board-level components. Clock sources available to the CCCs/PLLs include the internal RC and external crystal oscillators, an external clock source, or an internal signal. For systems dependent upon an external clock source, the RC oscillator serves as an excellent backup clock, ensuring your board never gets hung out to dry in the event of primary clock failure. Fusion increases system reliability by reducing clocking chip count and providing an integrated secondary clock source.



Fusion System Clocking

The Fusion real-time counter (RTC) includes a programmable 40-bit counter and match register (timer) that generates time-based match events. In addition to use models such as watchdog timer, device lifetime monitoring, and event timer, the RTC can be used to wake the Fusion device out of standby mode, enabling very low power modes of operation. The No-Glitch MUX (NGMUX) enables controlled switches between asynchronous clock domains. The device can switch to a slower clock frequency during periods of relative inactivity, reducing active power consumption.

Diagnostics/Prognostics

The ability to read back timestamped system parameters about board operation is invaluable in failure analysis. The Fusion on-chip Flash memory provides designers the ability to save and timestamp key system parameters such as current consumption of power rails, device temperatures, and voltage rail fluctuations. This data can be analyzed after failure to identify root cause and this can be an advantage for innovative designers who are looking to analyze system trends during operation. By analyzing how a particular parameter varies over the life of the board, it is possible to predict a failure before it occurs and repair the failure in a planned manner, rather than as an unplanned upset. Studies have shown that this behavior quickly improves system availability.

Remote and Local Communications

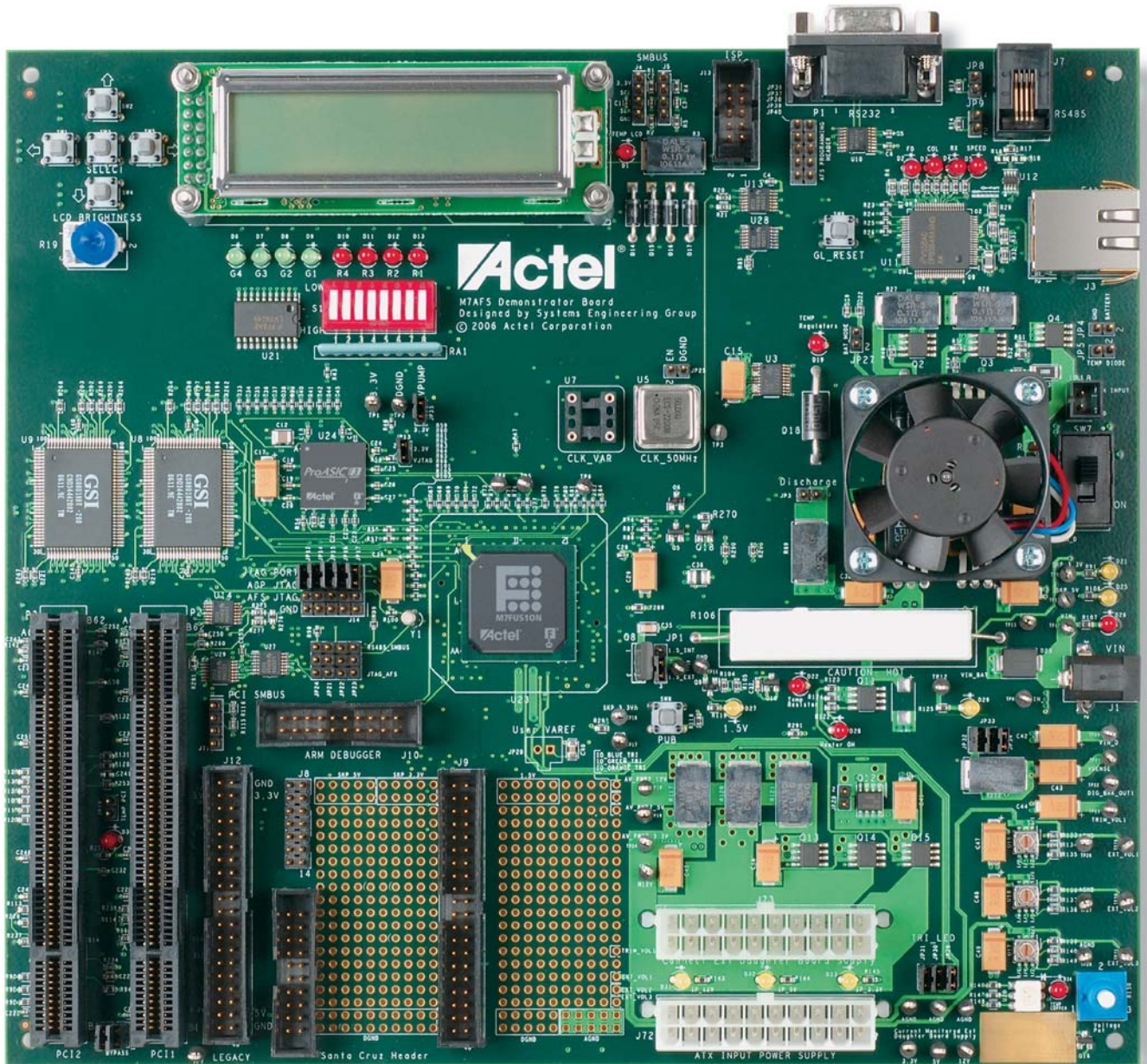
As a programmable device, Fusion supports a wide variety of communication protocols and implementations for both remote and local communication standards. Users can implement their own proprietary communication protocols or a number of communication IP cores available from Actel, including UART, I2C (IPMB-0 and IPMB-L), SPI, SMBus, PCI, 10/100, CAN, proprietary, and more.

These cores typically support slave and master modes. Actel also makes available a large number of GPIOs with many I/O standards supported.

Identification/Authentication

Security continues to be a primary concern for both users and developers. Fusion is designed with security in mind. As a single-chip solution, there is no communication between devices of any design files that could be intercepted and cloned. Backed with AES security, Fusion is secure from external tampering. Designers can implement secure “handshakes” or device authentication to ensure only authorized components are used within a system. This prevents the manufacturing of “knock-off” system cards or other devices that can affect system reliability, your reputation, or your bottom line.

Complete System Management Development Kit



The Actel System Management Development Kit provides an excellent platform for developing system management applications and/or applications with a microprocessor. The kit includes an ARM[®]-enabled Fusion device, a system management GUI, and a platform for systems that performs these functions:

- Power-up detection
- Power sequencing
- Thermal management
- Sleep modes
- System diagnostics
- Remote communications
- Clock generation and management

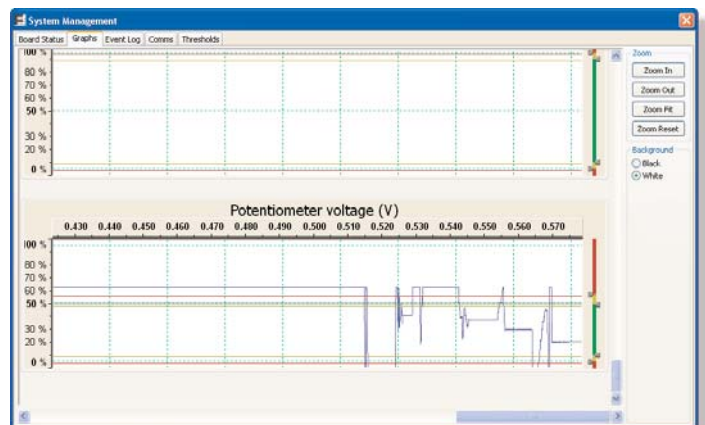
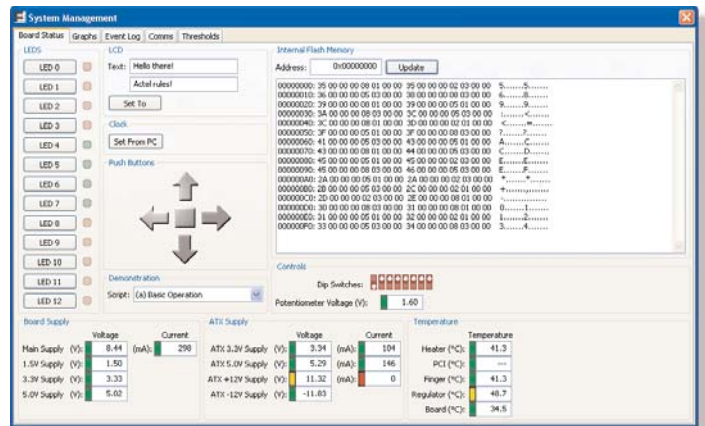
The board includes an M7AFS600 device, which is compatible with CoreMP7, Core8051, and other processors, as well as non-processor-based implementations. The kit's demonstration design uses the MicroC/OS-II on CoreMP7 with the system management GUI, which is multi-tabbed for board status, application data, IPMI data, and a graphical display of the monitored analog data. In addition, the GUI source code is available for custom modification.

The system management GUI is multi-tabbed:

- Board status
- Application data
- IPMI data
- Graphical display of analog data

The GUI helps users to:

- Monitor power supplies
- Monitor temperature sensors
- Set LEDs and text for display
- Set and read the RTC
- Display embedded Flash contents



Actel Fusion Product Table

Fusion Devices		AFS090	AFS250	AFS600	AFS1500
ARM-Enabled Fusion Devices	CoreMP7 ²			M7AFS600	
	Cortex-M1 ³		M1AFS250	M1AFS600	M1AFS1500
General	System Gates	90,000	250,000	600,000	1,500,000
	Tiles (D-Flip-Flops)	2,304	6,144	13,824	38,400
	Secure (AES) ISP	Yes	Yes	Yes	Yes
	PLLs	1	1	2	2
	Globals	18	18	18	18
Memory	Flash Memory Blocks (2 Mbits)	1	1	2	4
	Total Flash Memory Bits (Mbits)	2	2	4	8
	FlashROM Bits (kbits)	1	1	1	1
	RAM Blocks (4,608 bits)	6	8	24	60
	RAM (kbits)	27	36	108	270
Analog and I/Os	Analog Quads	5	6	10	10
	Analog Input Channels	15	18	30	30
	Gate Driver Outputs	5	6	10	10
	I/O Banks (+ JTAG)	4	4	5	5
	Maximum Digital I/Os	75	114	172	252
	Analog I/Os	20	24	40	40
I/O: Single-/Double-Ended (Analog)	QN108	37/9 (16)			
	QN180	60/16 (20)	65/15 (24)		
	PQ208		93/26 (24)	95/46 (40)	
	FG256	75/22 (20)	114/37 (24)	119/58 (40)	119/58 (40)
	FG484			172/86 (40)	223/109 (40)
	FG676				252/126 (40)

Notes: ¹Please refer to the Actel website and datasheet for the latest device information. ²Refer to the CoreMP7 datasheet for more information. ³Refer to the Cortex-M1 product brief for more information.

For more information regarding **Actel Fusion System Management Solutions**, please contact your local **Actel** sales representative.



Actel Corporation

2061 Stierlin Court
Mountain View, CA
94043-4655 USA
Phone 650.318.4200
Fax 650.318.4600

Actel Europe Ltd.

River Court, Meadows Business Park
Station Approach, Blackwater
Camberley Surrey GU17 9AB
United Kingdom
Phone +44 (0) 1276 609 300
Fax +44 (0) 1276 607 540

Actel Japan

EXOS Ebisu Building 4F
1-24-14 Ebisu Shibuya-ku
Tokyo 150, Japan
Phone +81.03.3445.7671
Fax +81.03.3445.7668
www.jp.actel.com

Actel Hong Kong

Suite 2114, Two Pacific Place
88 Queensway, Admiralty
Hong Kong
Phone +852 2185 6460
Fax +852 2185 6488
www.actel.com.cn